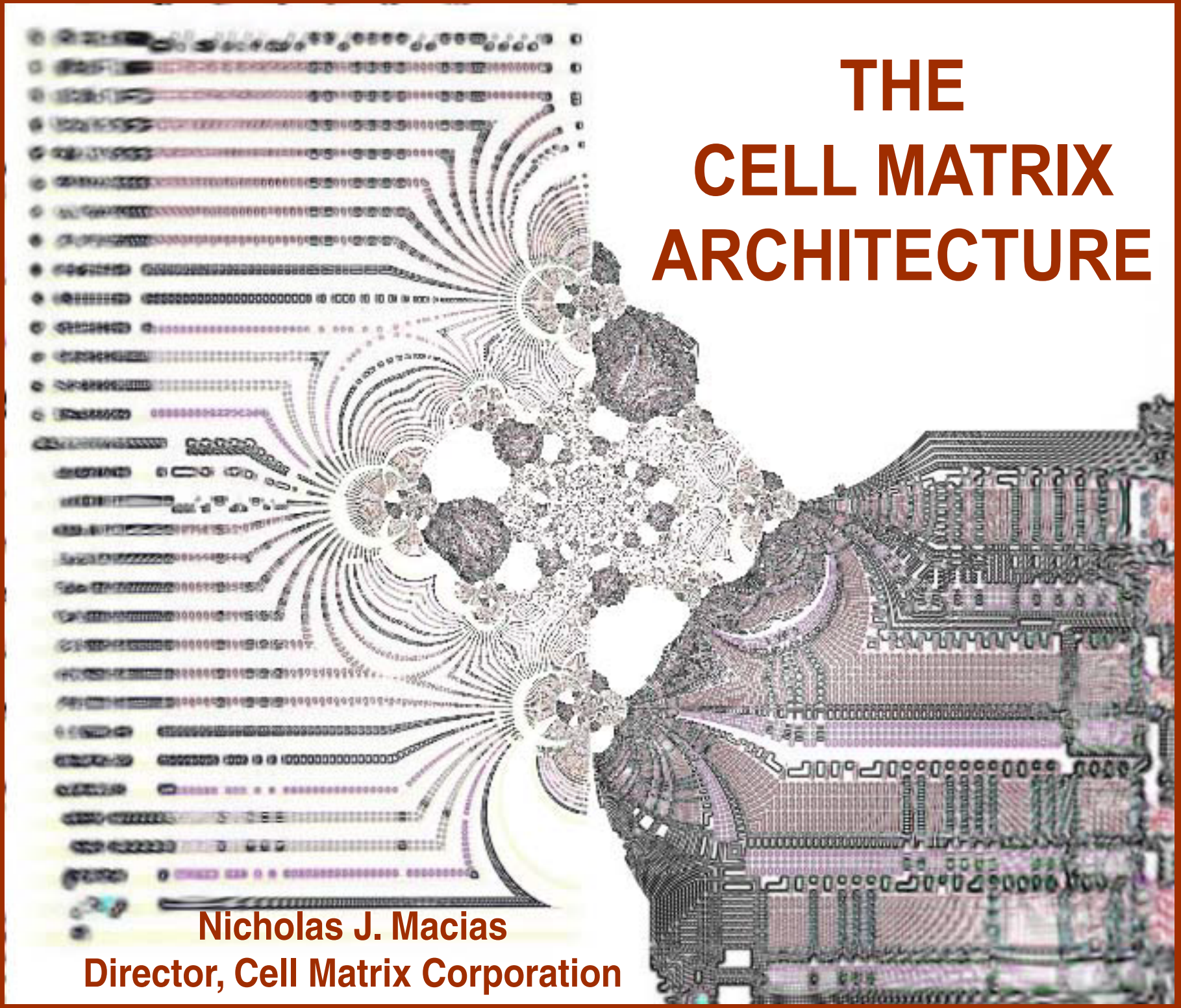
THE CELL MATRIX ARCHITECTURE



Nicholas J. Macias
Director, Cell Matrix Corporation

TALK OVERVIEW

- Architectural Overview

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- D-Mode Operations (Static Circuits)

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- D-Mode Operations (Static Circuits)
- C-Mode Operations (Dynamic Circuits)

TALK OVERVIEW

- Architectural Overview
- D-Mode Operations (Static Circuits)
- C-Mode Operations (Dynamic Circuits)
- Applications to Manufacturing

WHAT IS A CELL MATRIX?

ARCHITECTURAL FEATURES

- Composed of simple, identical, general-purpose, reconfigurable atomic units ("Cells")

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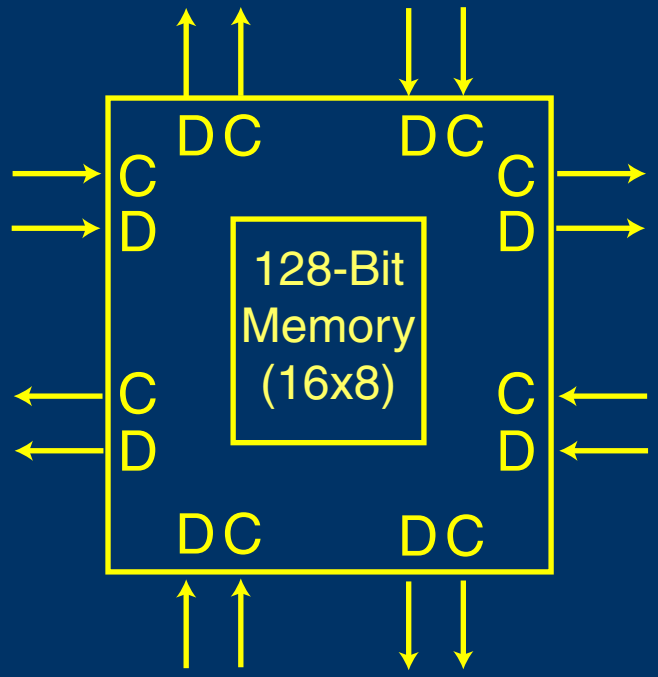
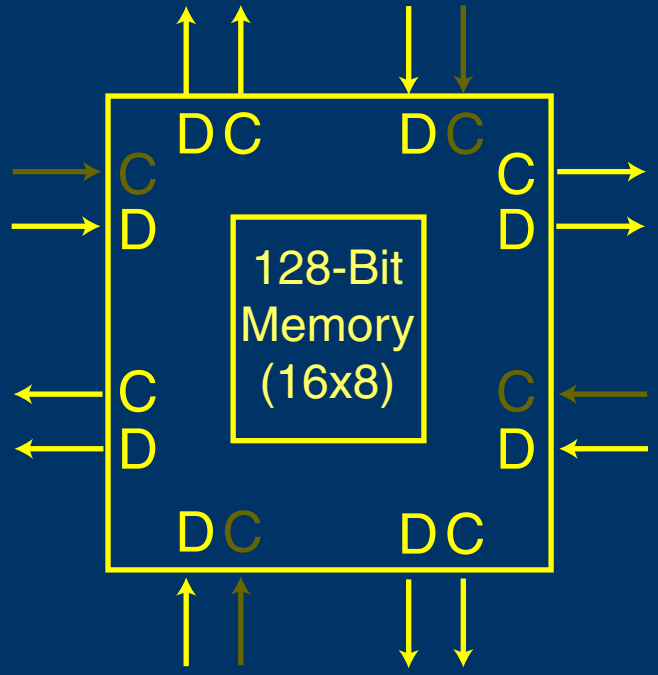
- Composed of simple, identical, general-purpose, reconfigurable atomic units ("Cells")
- Regular interconnect; Extremely scalable
- Self Configurable

Atomic Unit of Cell Matrix



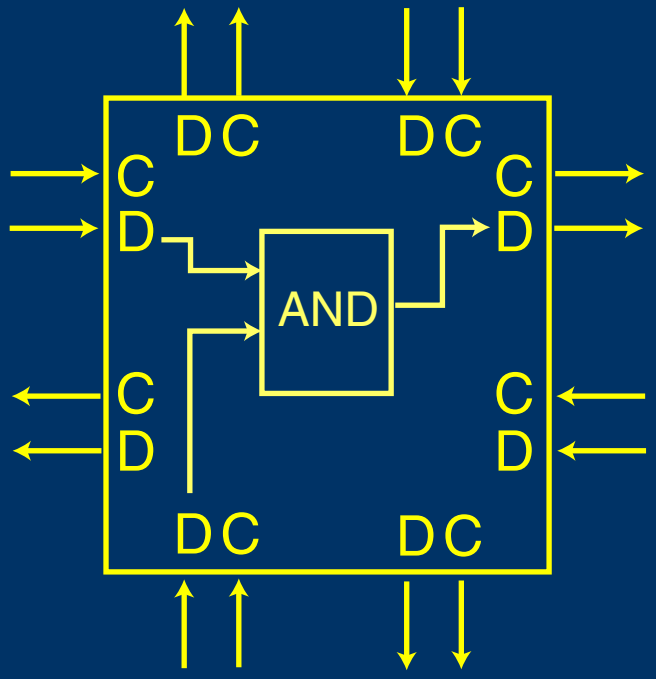
Atomic Unit of Cell Matrix



Cell Matrix Truth Table

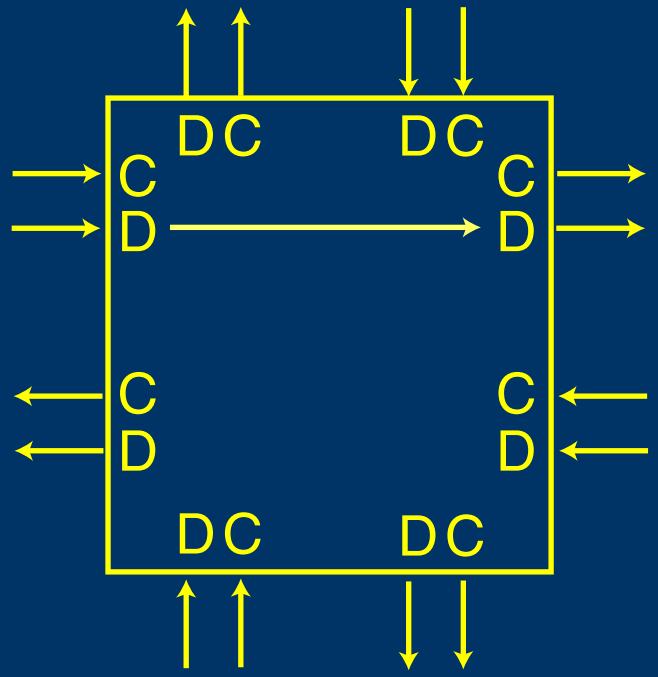
INPUTS				OUTPUTS							
DN	DS	DW	DE	CN	CS	CW	CE	DN	DS	DW	DE
0	0	0	0	0	0	0	0	0	1	0	0
0	0	0	1	0	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	0	1	0	1
0	0	1	1	0	0	0	0	1	1	0	1
0	1	0	0	0	0	0	0	0	0	1	0
0	1	0	1	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	0	0	0	1	1
0	1	1	1	0	0	0	0	1	0	1	1
1	0	0	0	0	0	0	0	0	1	0	0
1	0	0	1	0	0	0	0	0	1	0	0
1	0	1	0	0	0	0	0	0	1	0	1
1	0	1	1	0	0	0	0	1	1	0	1
1	1	0	0	0	0	0	0	1	0	1	0
1	1	0	1	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1	1
1	1	1	1	0	0	0	0	0	0	1	1

Cells Implement Simple Logic Functions



$DE_{out} = DS_{in}.AND.DW_{in}$

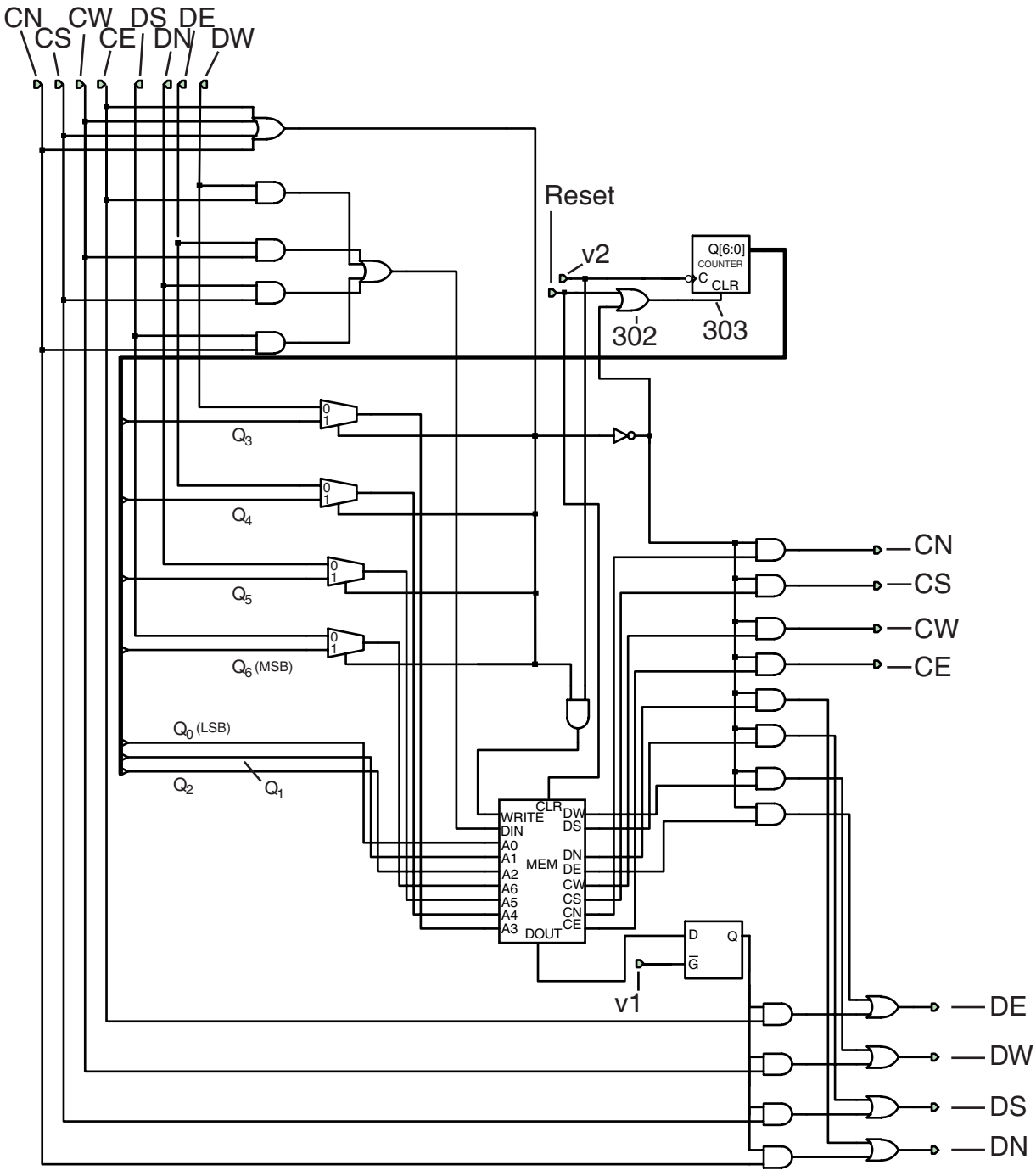
Sometimes Very Simple

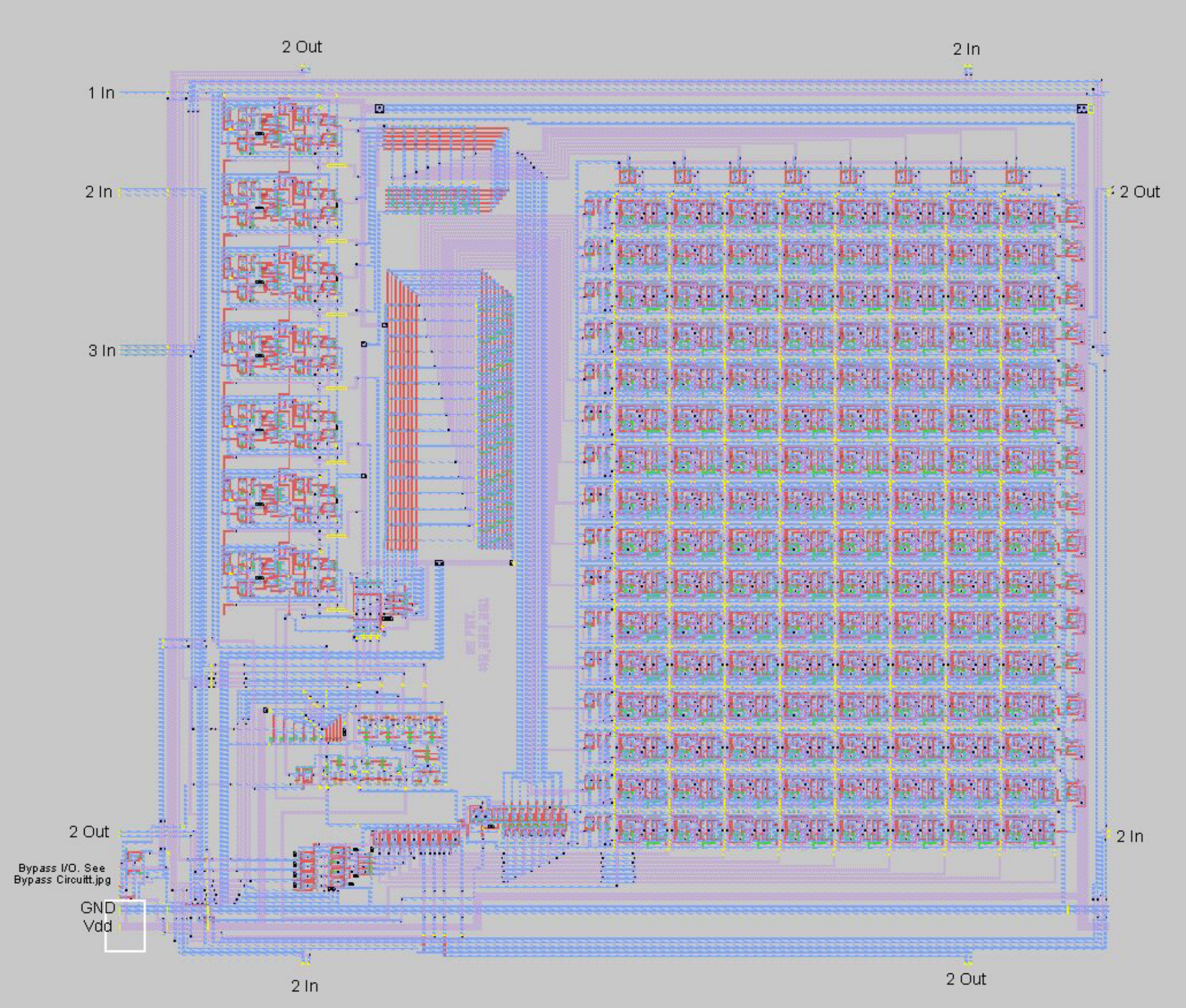


$DE_{out} = DW_{in}$

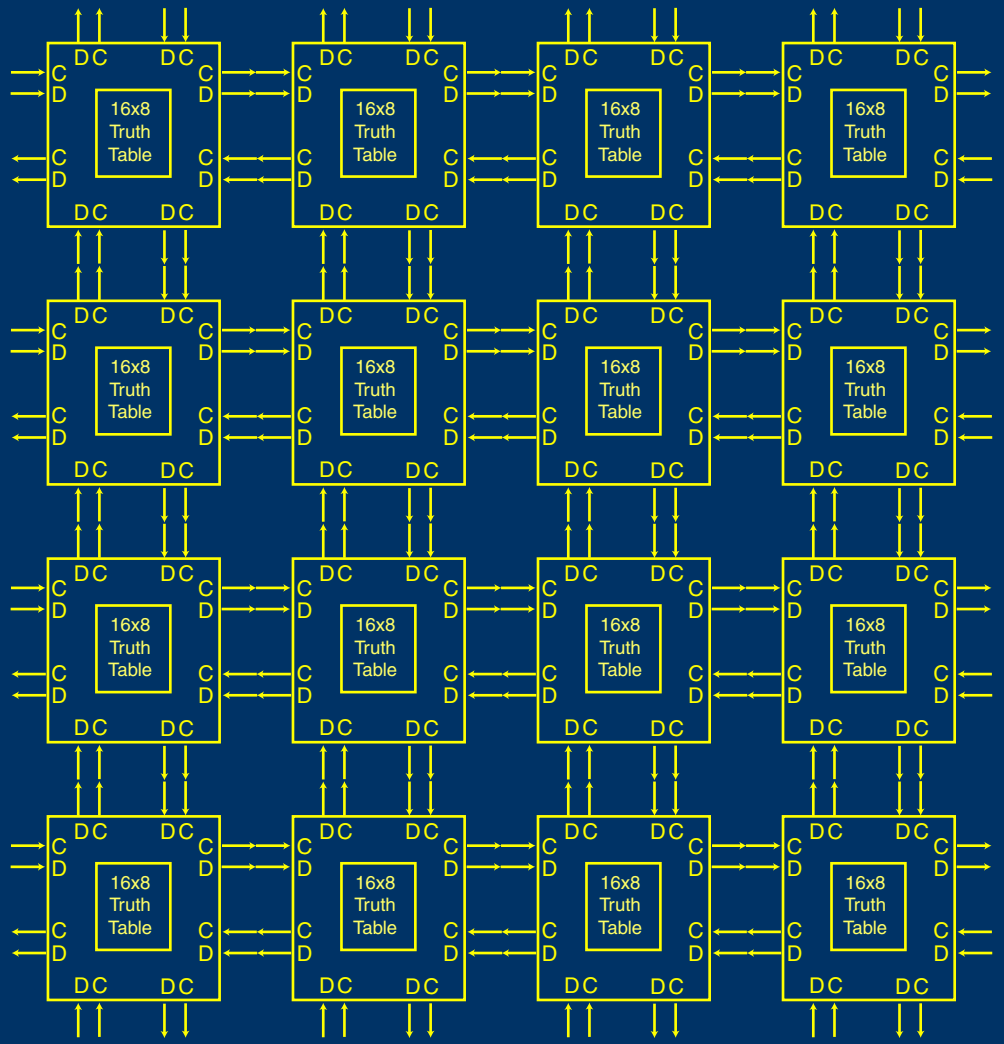
Truth Table for DW->DE

DN	DS	DW	DE	CN	CS	CW	CE	DN	DS	DW	DE
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	1
0	0	1	1	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	1
0	1	1	1	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	1
1	0	1	1	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	1
1	1	1	1	0	0	0	0	0	0	0	1


CN
CS
CW
CE
DS
DN
DE
DW
Reset
v2
Q[6:0]
COUNTER
C
CLR
302
303
Q3
Q4
Q5
Q6 (MSB)
Q0 (LSB)
Q2
Q1
WRITE
DIN
A0
A1
A2
A6
A5
A4
A3
MEM
DOUT
CLR
DW
DS
DN
DE
CW
CS
CN
CE
D
Q
G
v1
CN
CS
CW
CE
DE
DW
DS
DN

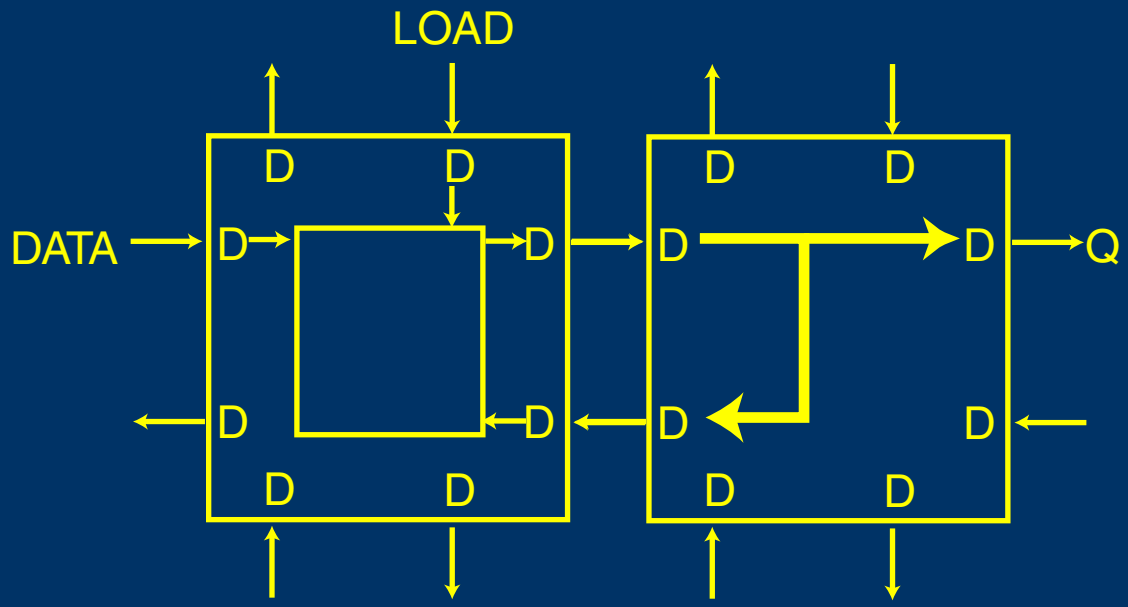

2 Out
2 In
1 In
2 In
2 Out
3 In
2 Out
2 In
Bypass I/O. See
Bypass Circuitt.jpg
GND
Vdd
2 In
2 Out

Tiling of Cells



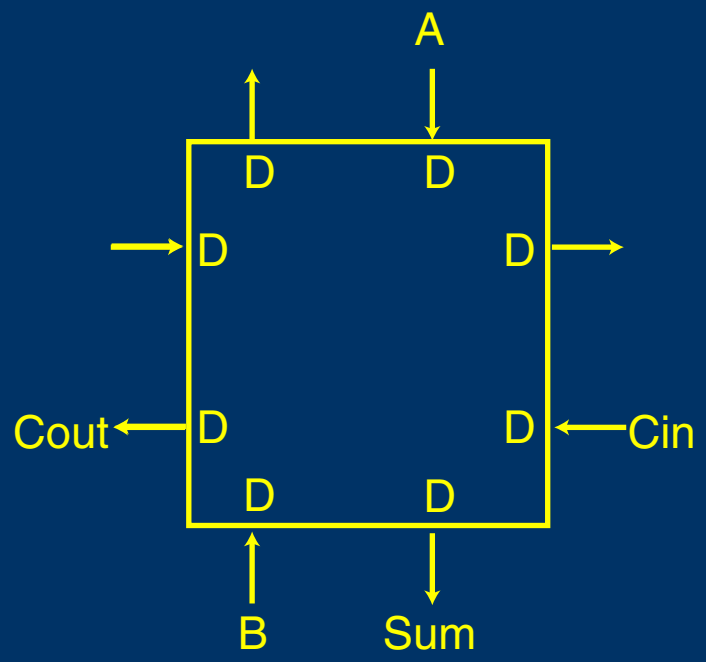
Cells work together to perform higher-order functions

D-FLIP FLOP

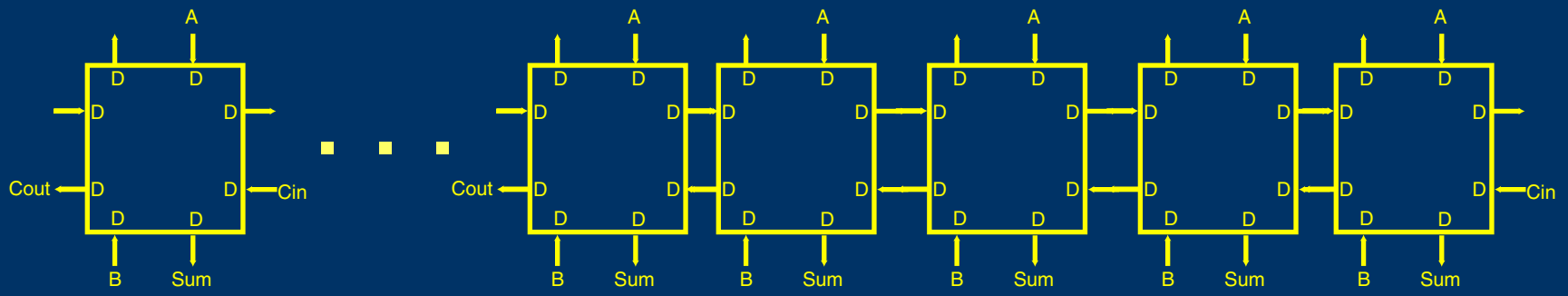


$$DW_{out}=(DN_{in}.DW_{in})+(\overline{DN}_{in}.DE_{in})$$

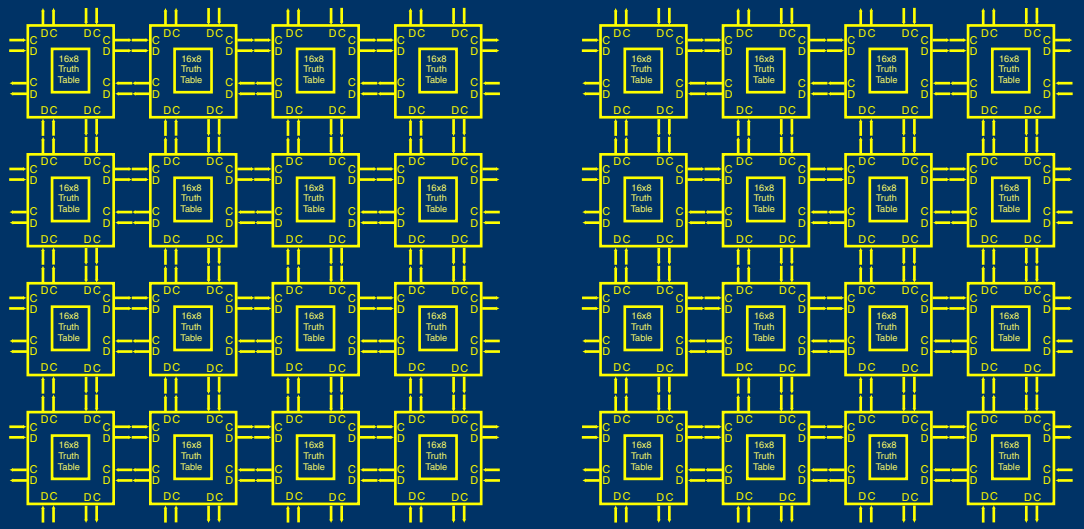
ONE-BIT ADDER



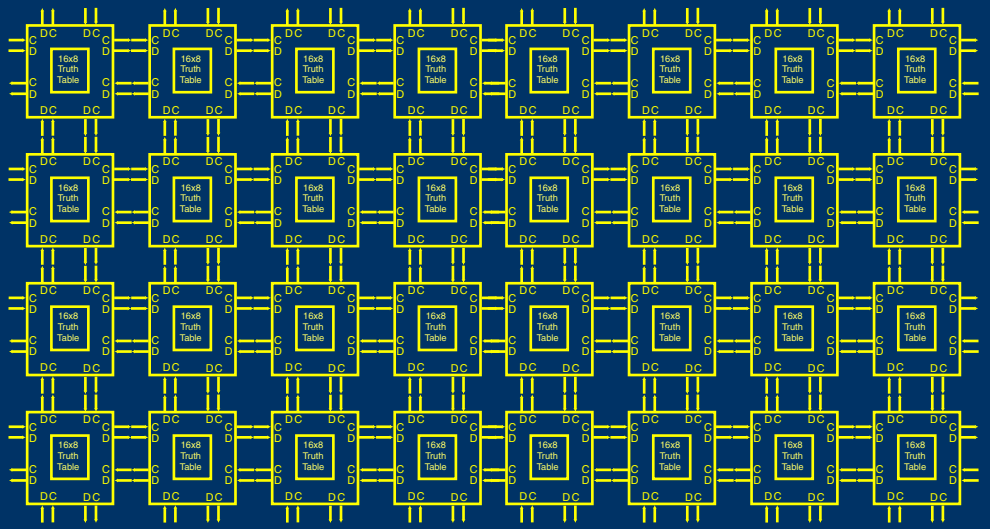
16-BIT ADDER



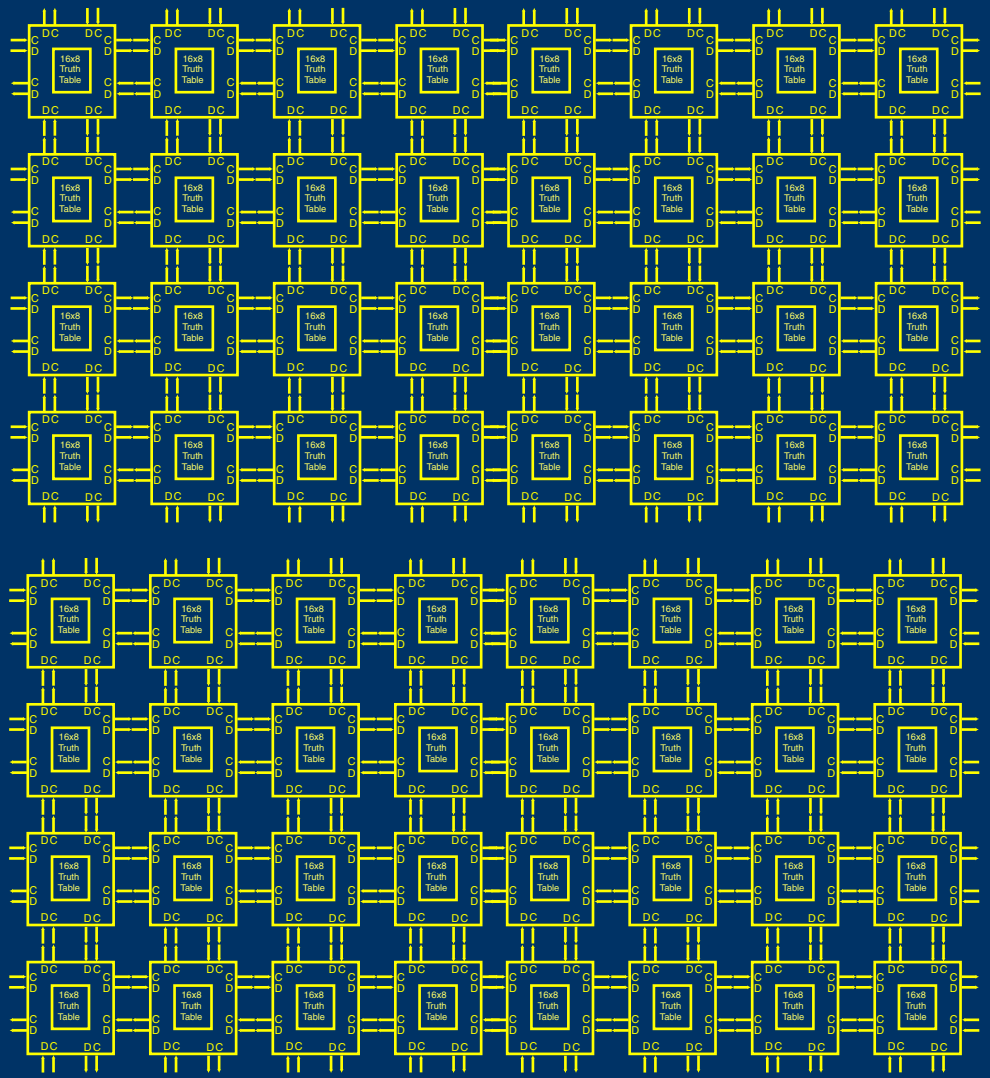
Scaling of the Matrix



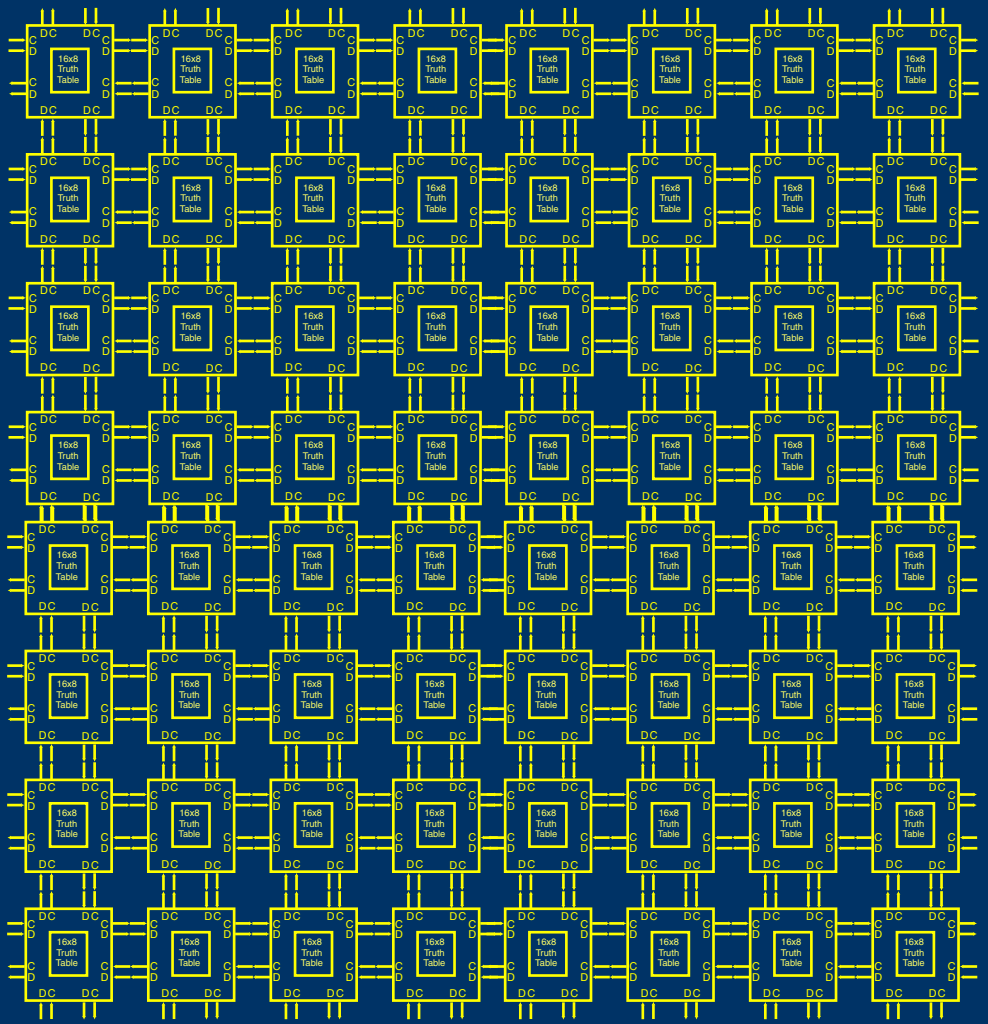
Scaling of the Matrix



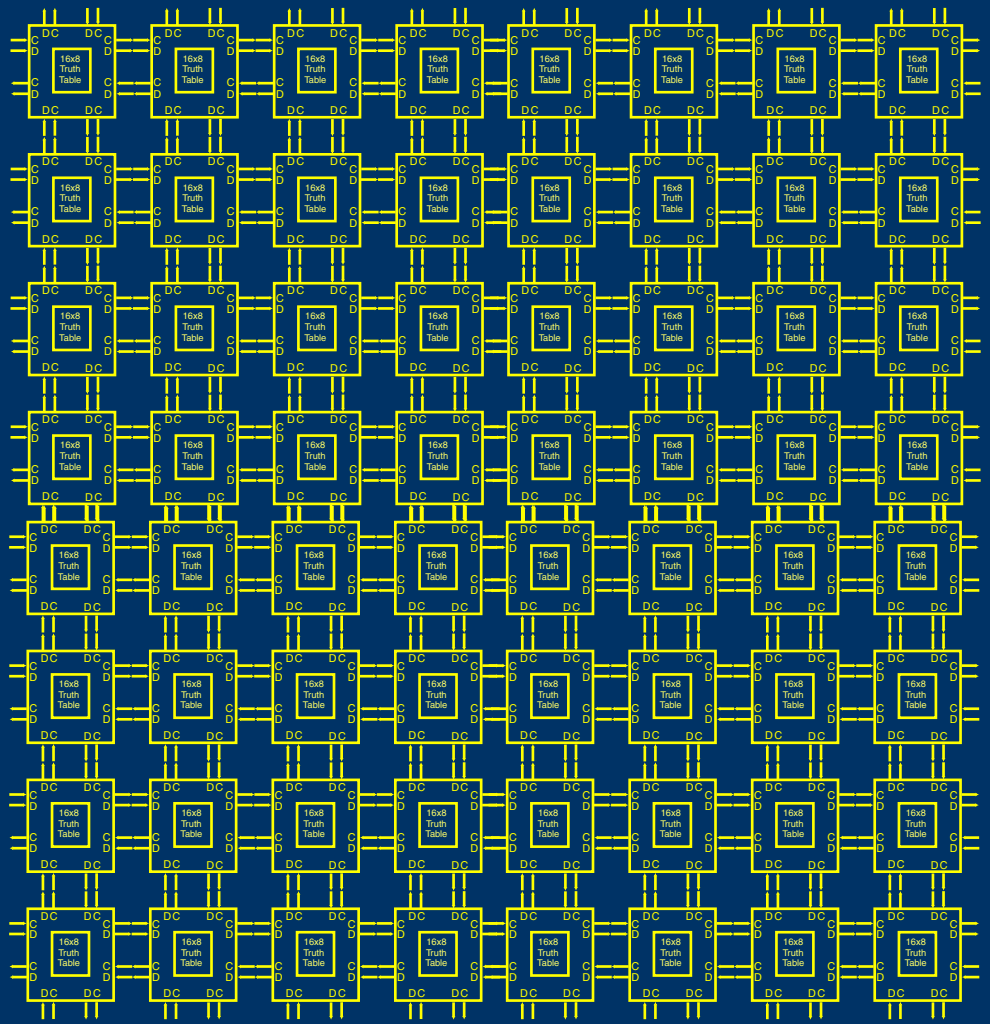
Scaling of the Matrix



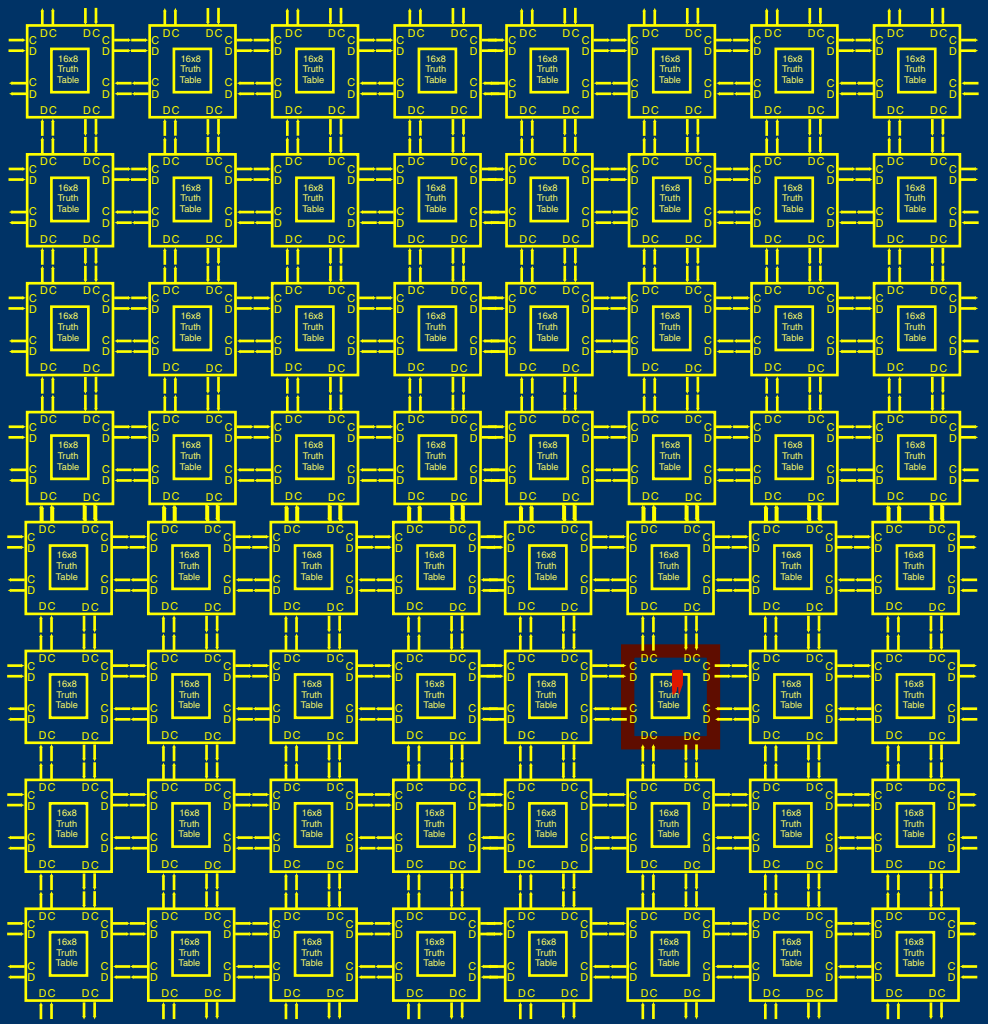
Scaling of the Matrix



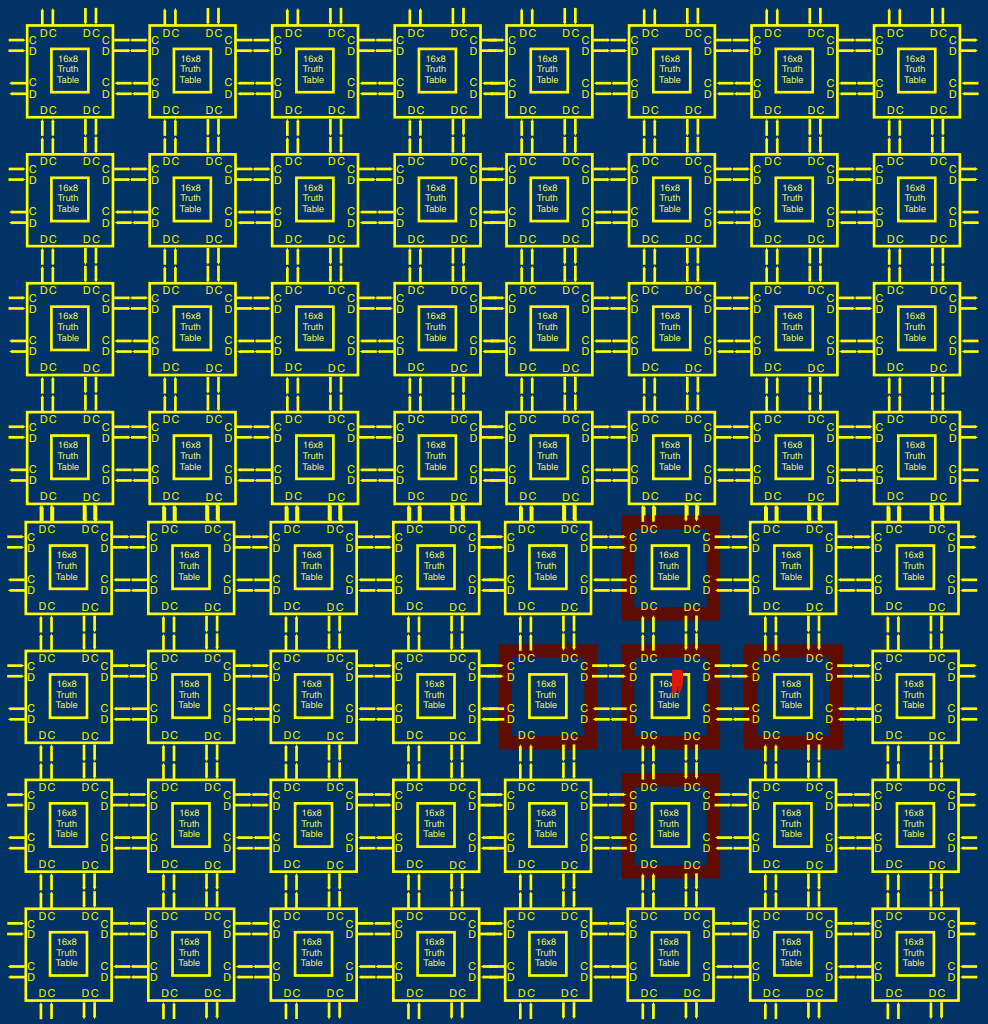
FAULT ISOLATION



FAULT ISOLATION

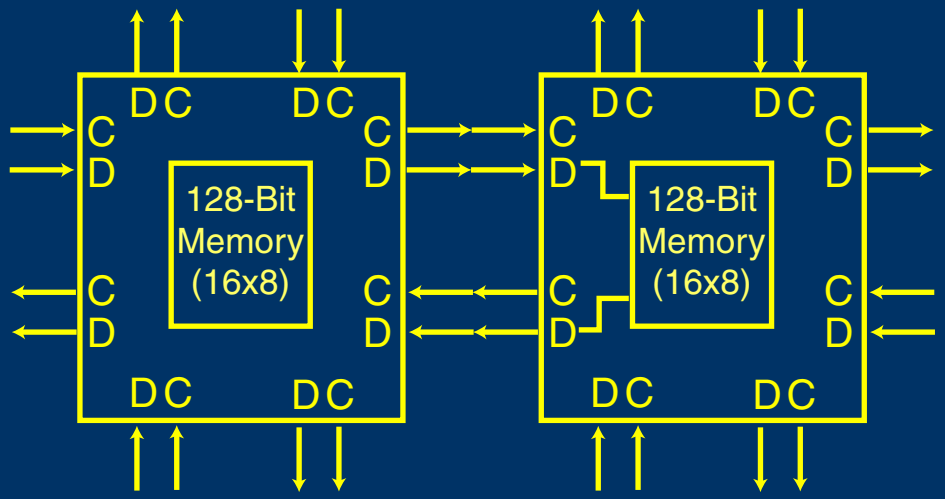


FAULT ISOLATION

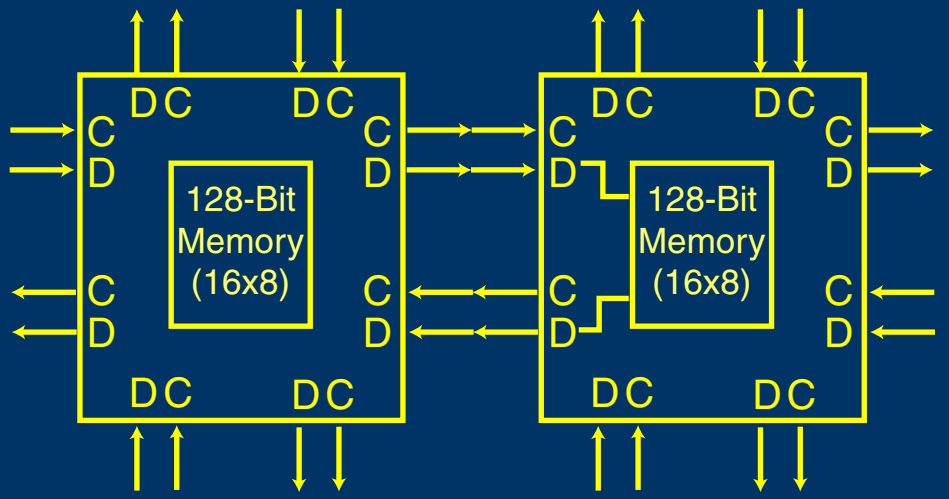


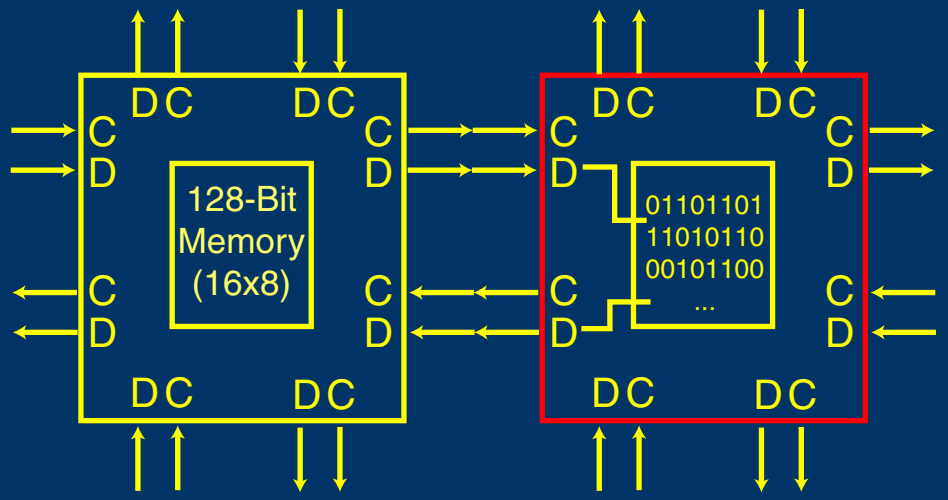
How are Cells Configured in a Cell Matrix?

So Far...



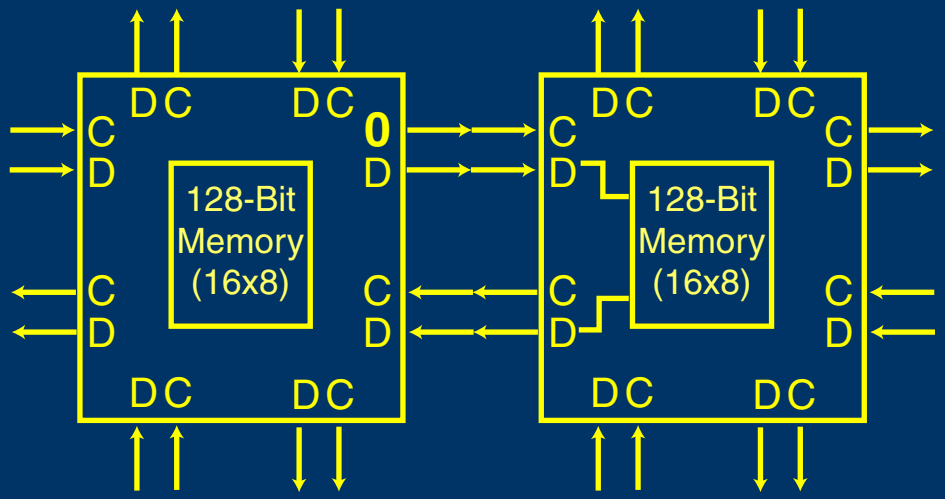
There is a Dual Mode



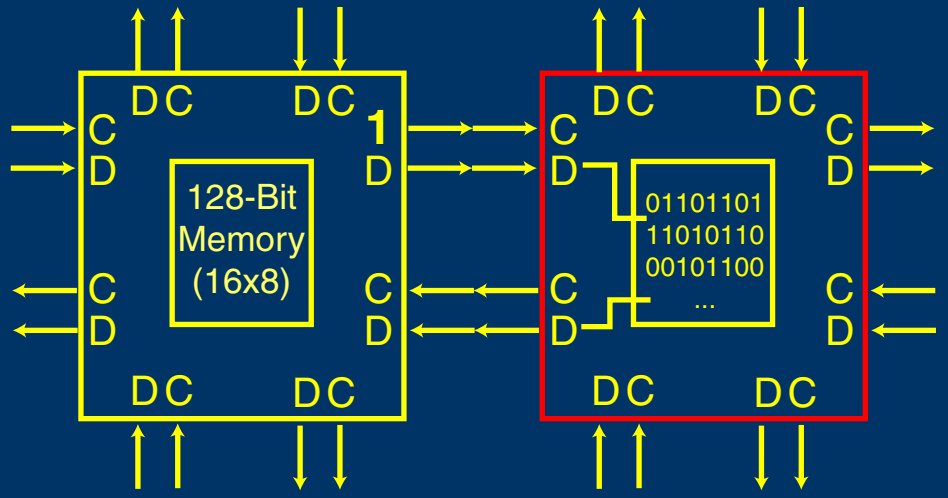


C-Mode is Indicated by Setting a C Input to1

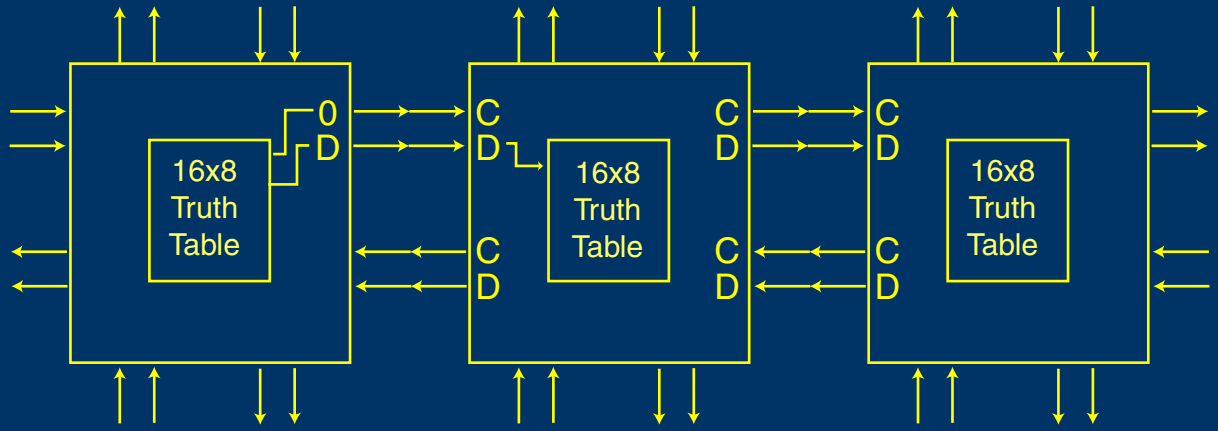
D-Mode:
Cells Exchange DATA



C-Mode:
Cells Exchange CODE



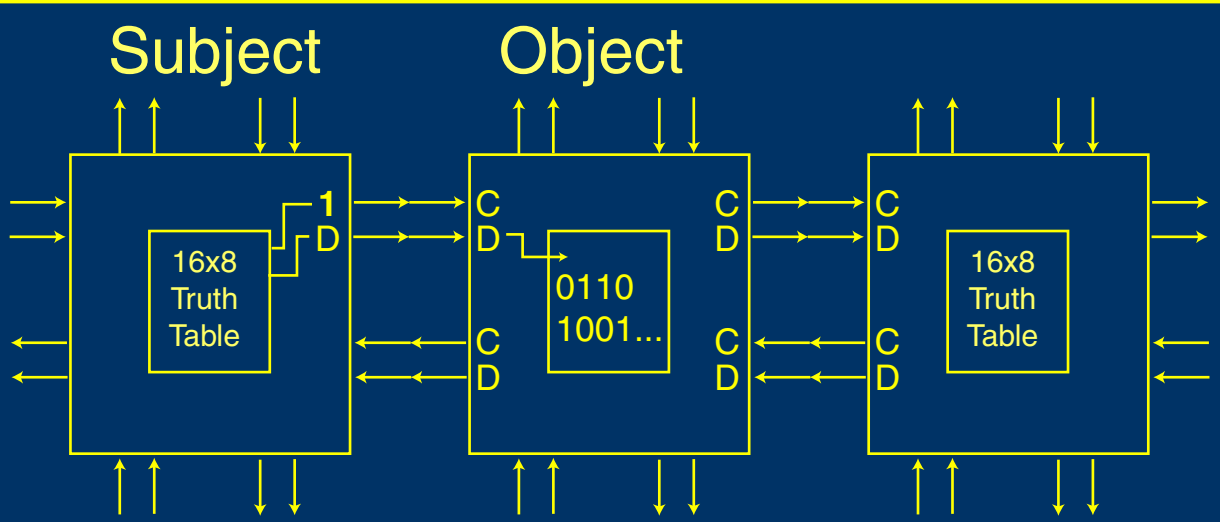
X May Pass Data to Y



X Y Z

Y is in D Mode

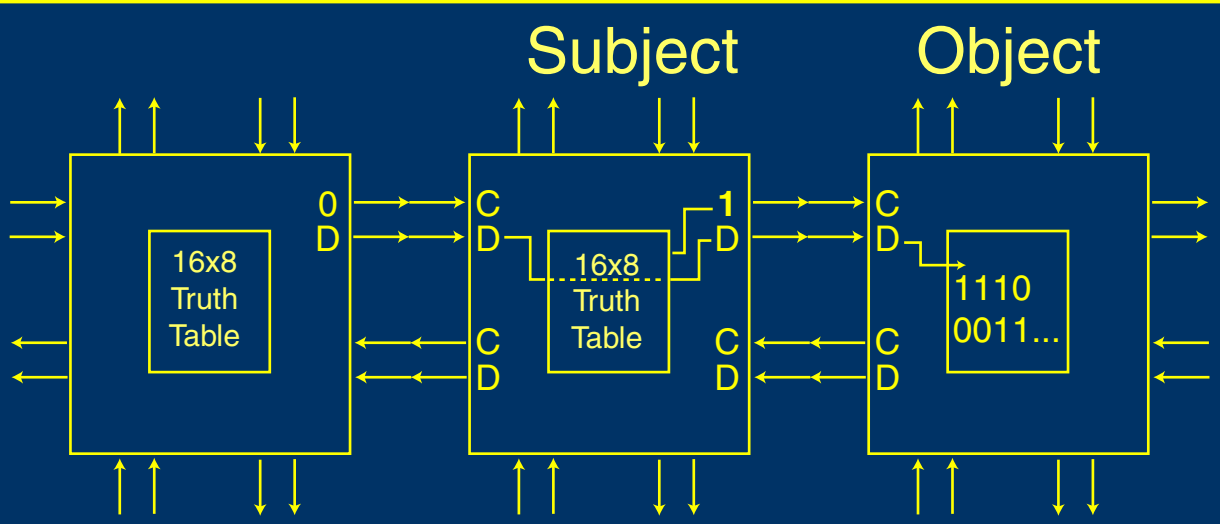
X May Configure Y



X Y Z

Y is in C Mode

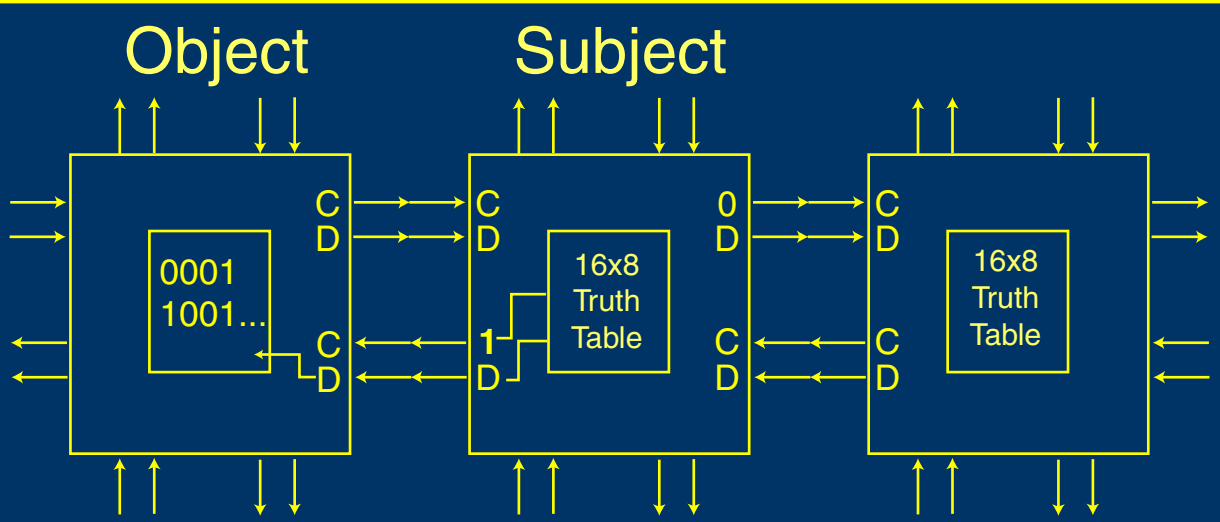
Y May Then Configure Z



X Y Z

Z is in C Mode

Or Y May Reconfigure X



X is in C Mode

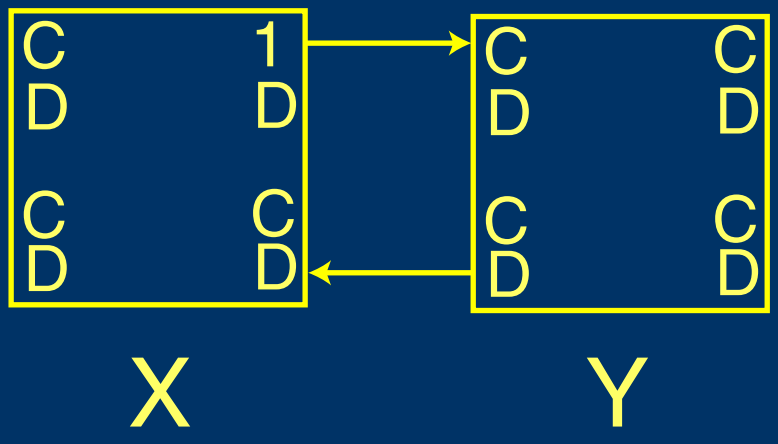
SELF DUALITY

There is a perfect interchangability between the subject and object of configuration

SELF CONFIGURABILITY

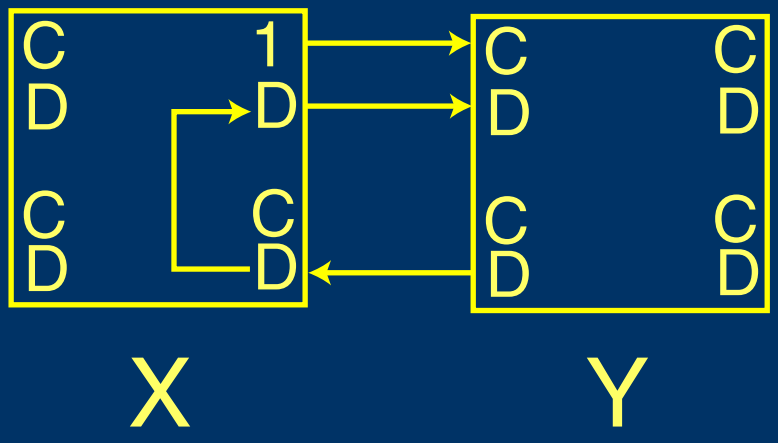
The Cell Matrix is able to read, modify and write its own configuration information.

Cell Reader



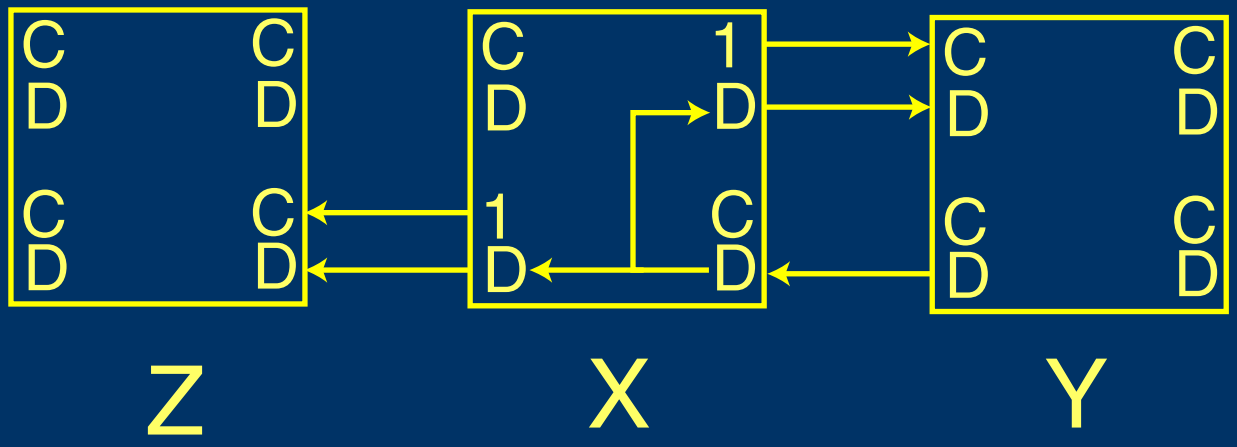
X is reading Y's Truth Table

Non-Destructive Cell Reader



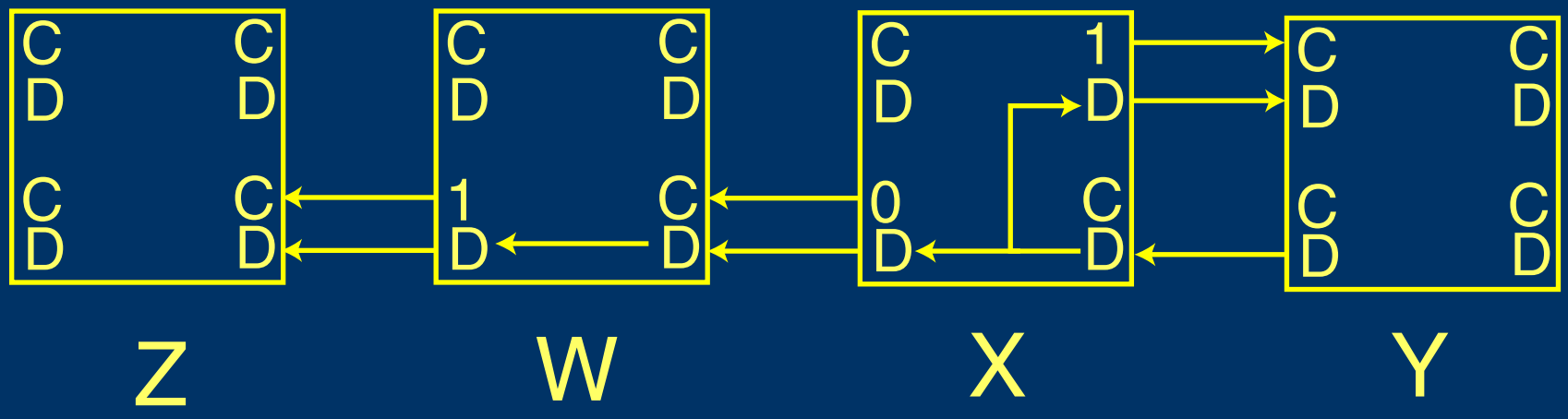
X is reading Y's Truth Table
and copying it back to Y

Cell Replicator



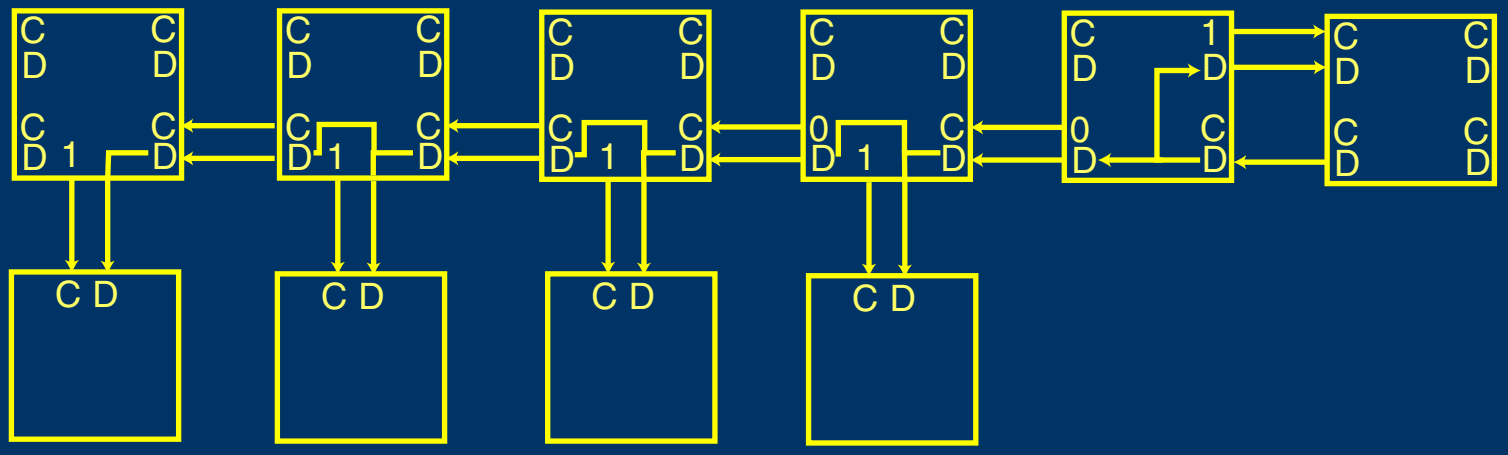
X is reading Y's Truth Table,
copying it back to Y,
and also copying it to Z

Remote Cell Replicator



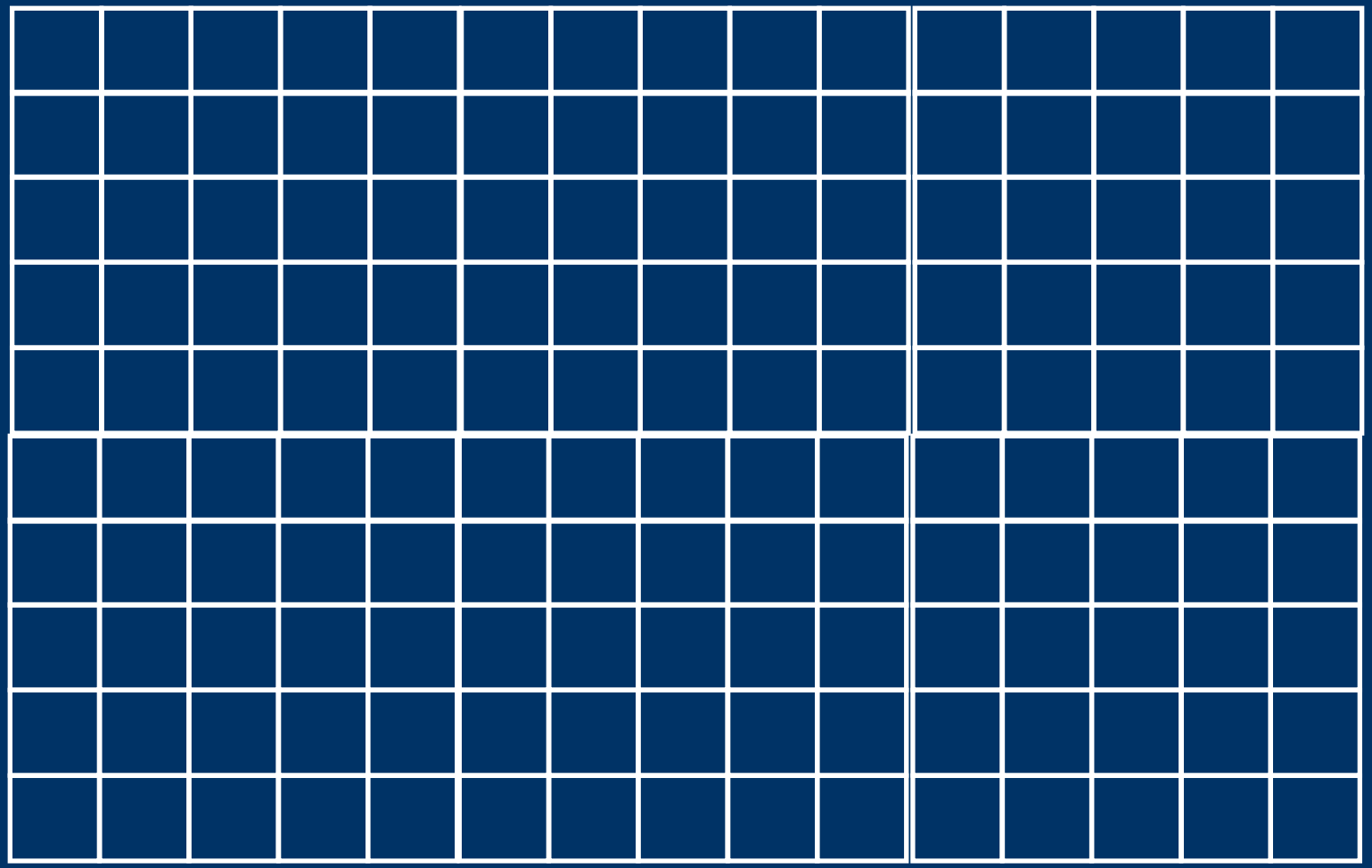
X is reading Y's Truth Table,
copying it back to Y,
and also copying it to Z

Medusa Circuit

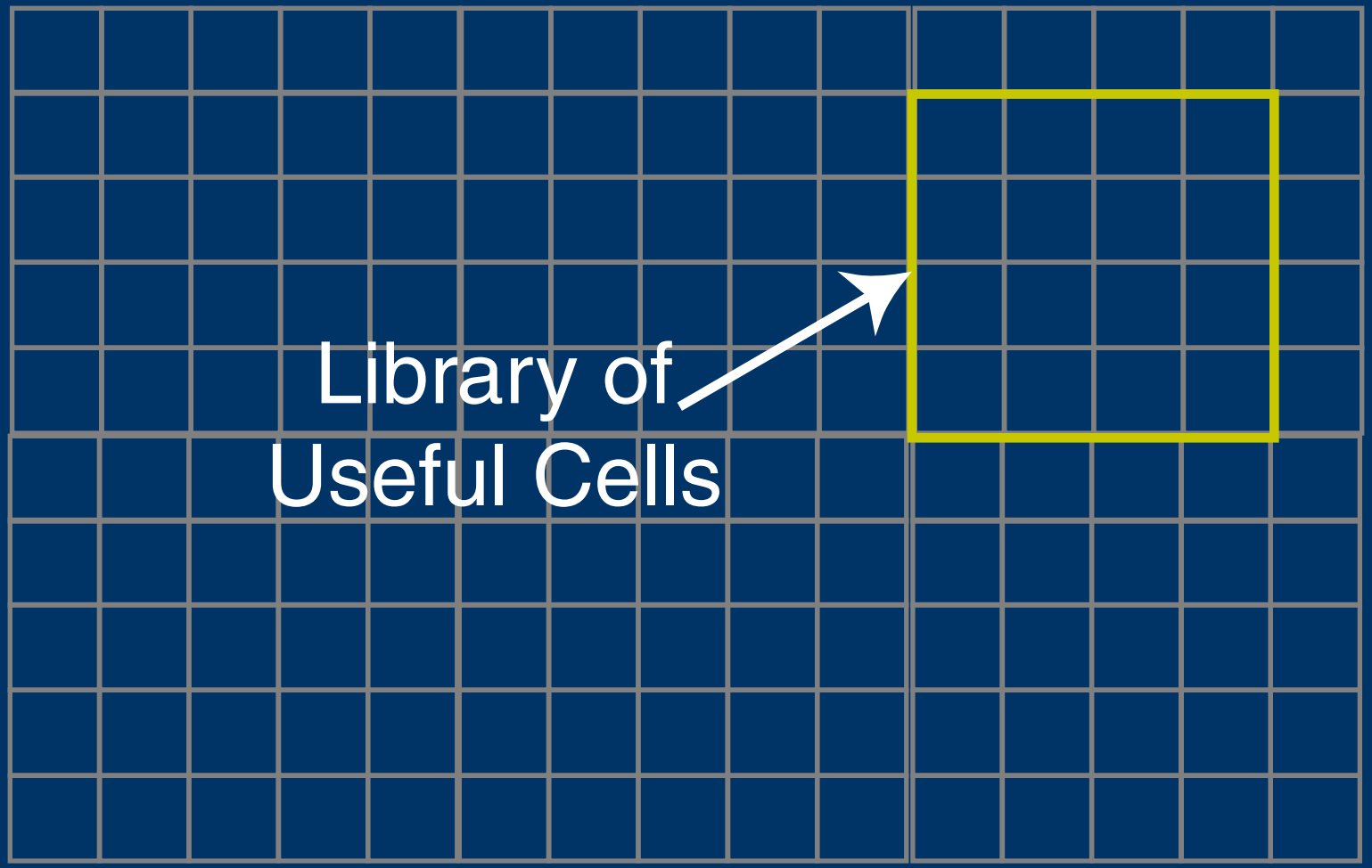


FOUR CELLS CONFIGURED
SIMULTANEOUSLY

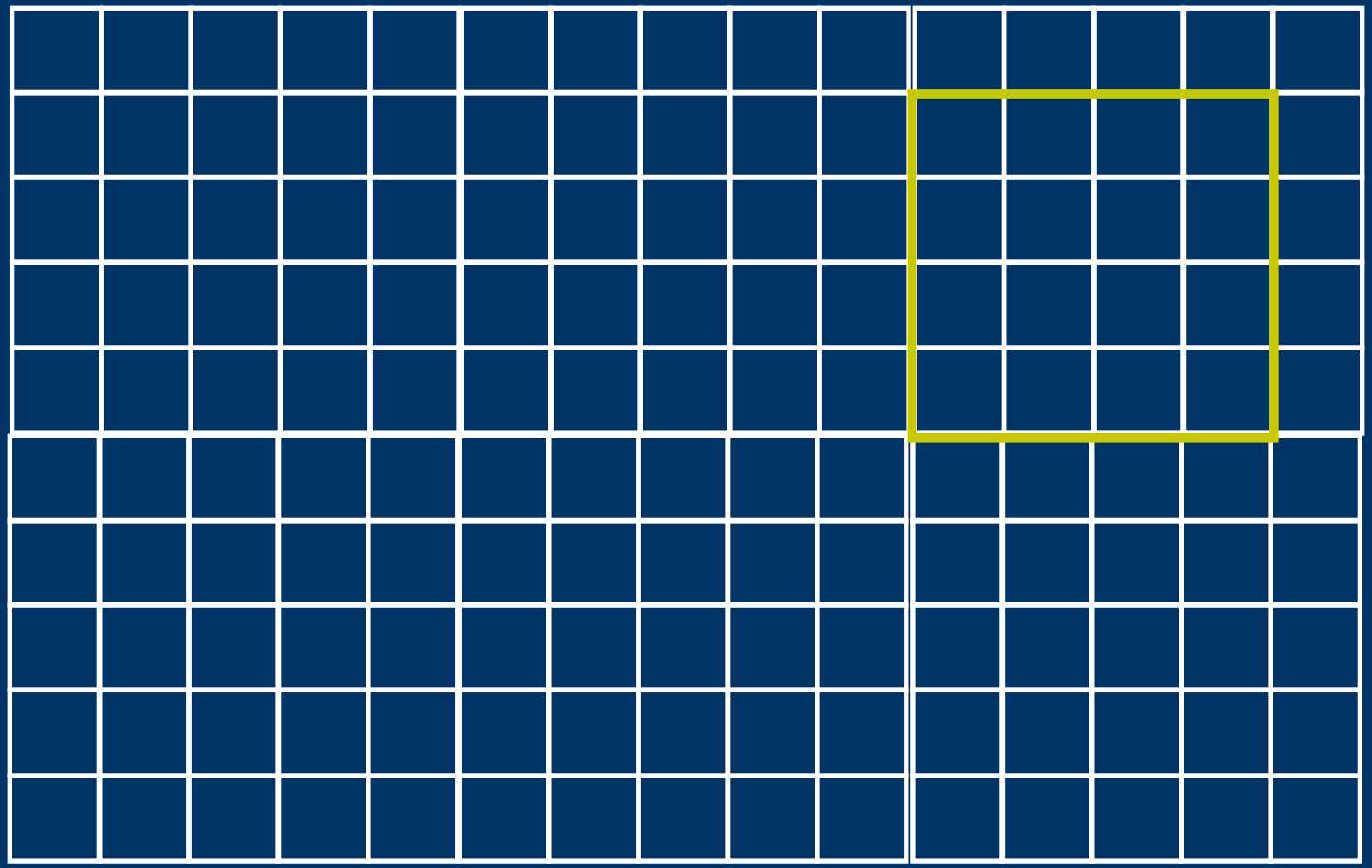
EXAMPLE: HARDWARE LIBRARY



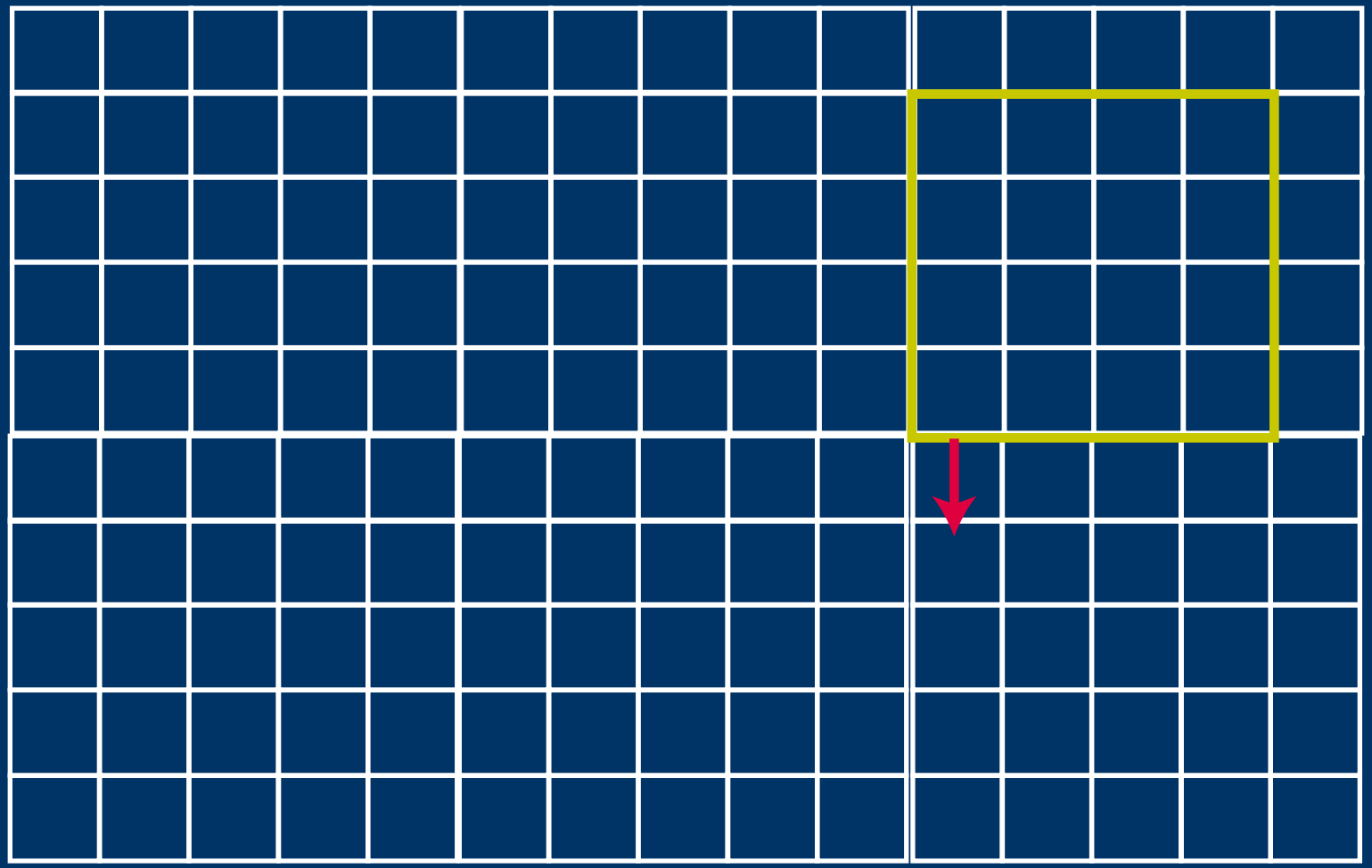
EXAMPLE: HARDWARE LIBRARY



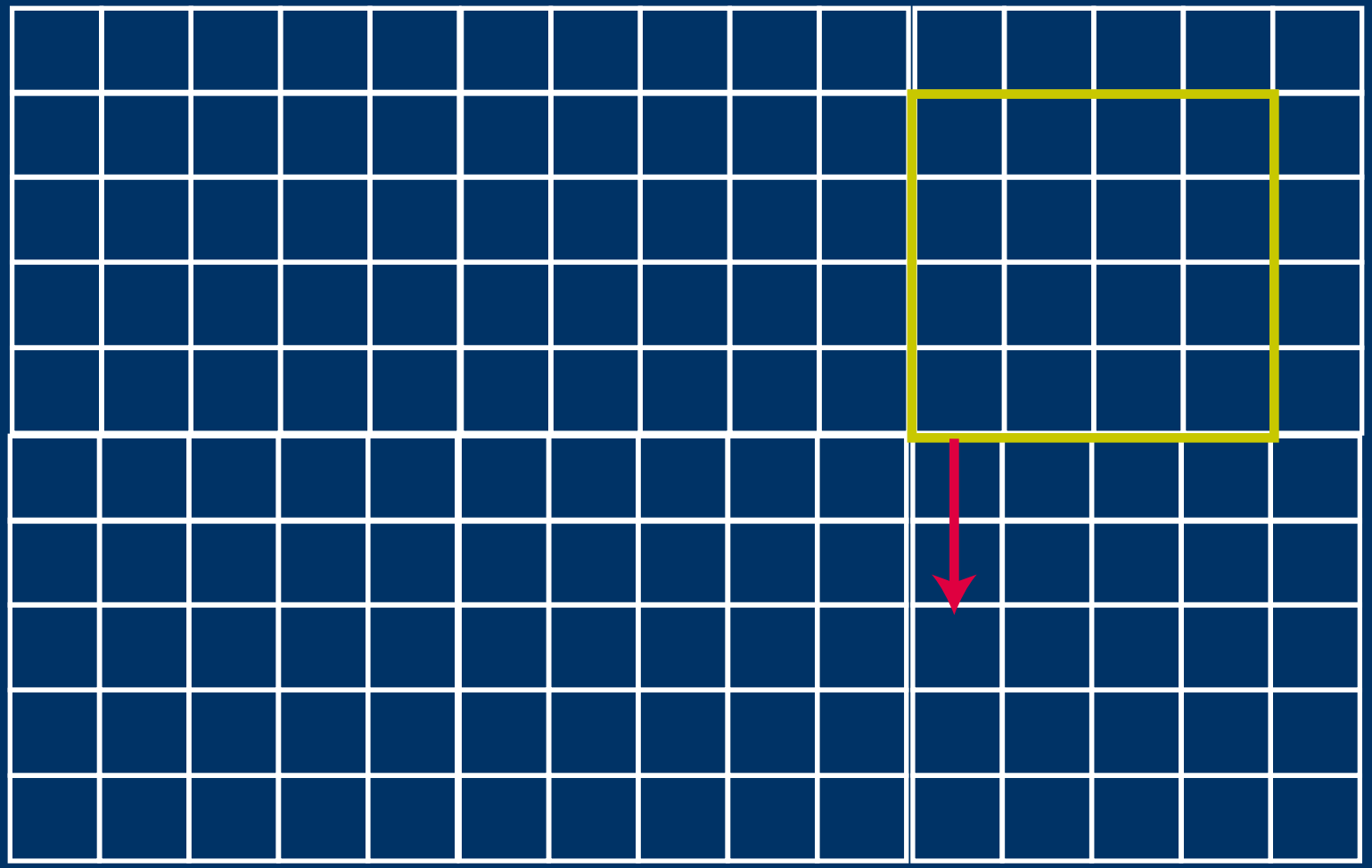
EXAMPLE: HARDWARE LIBRARY



EXAMPLE: HARDWARE LIBRARY



EXAMPLE: HARDWARE LIBRARY



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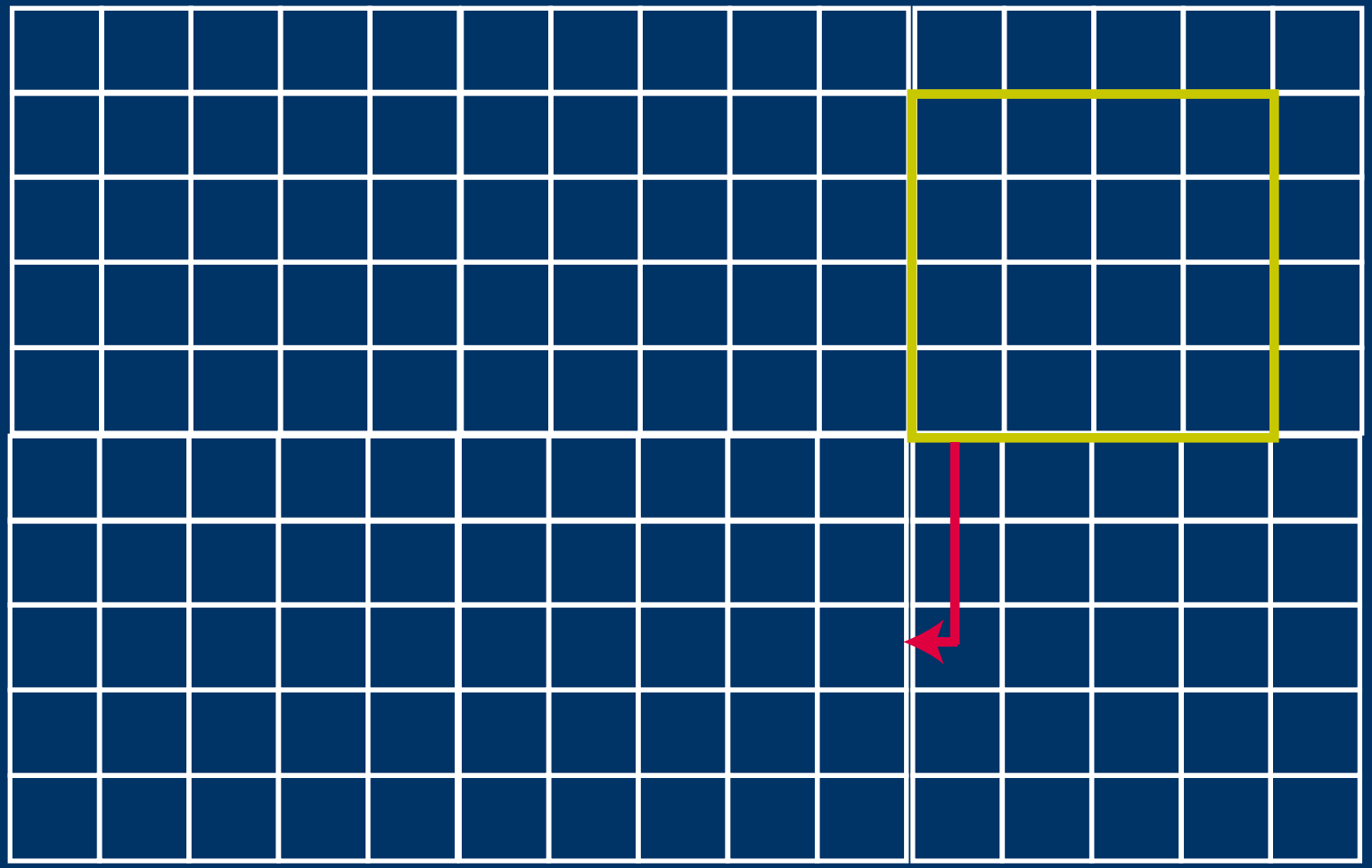
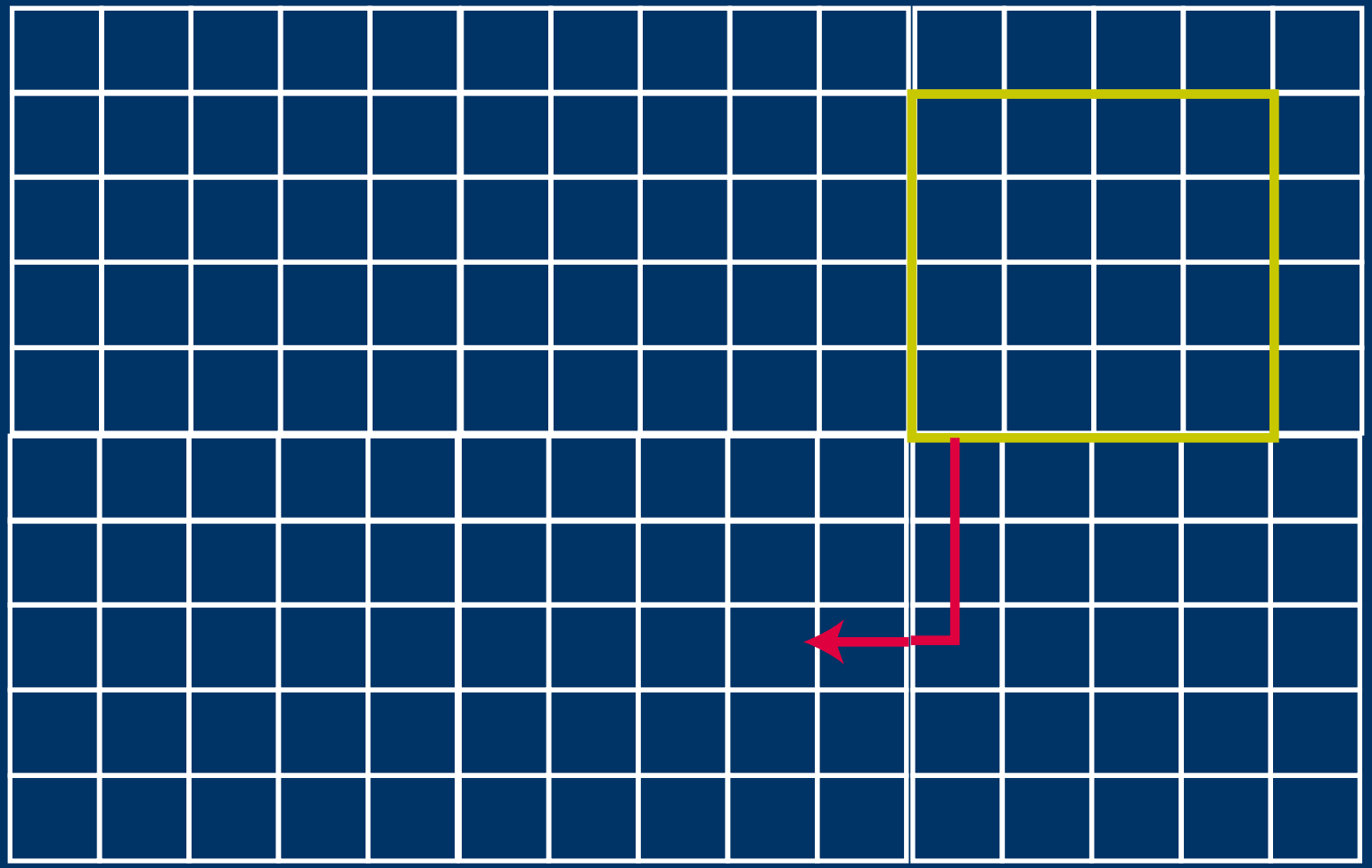
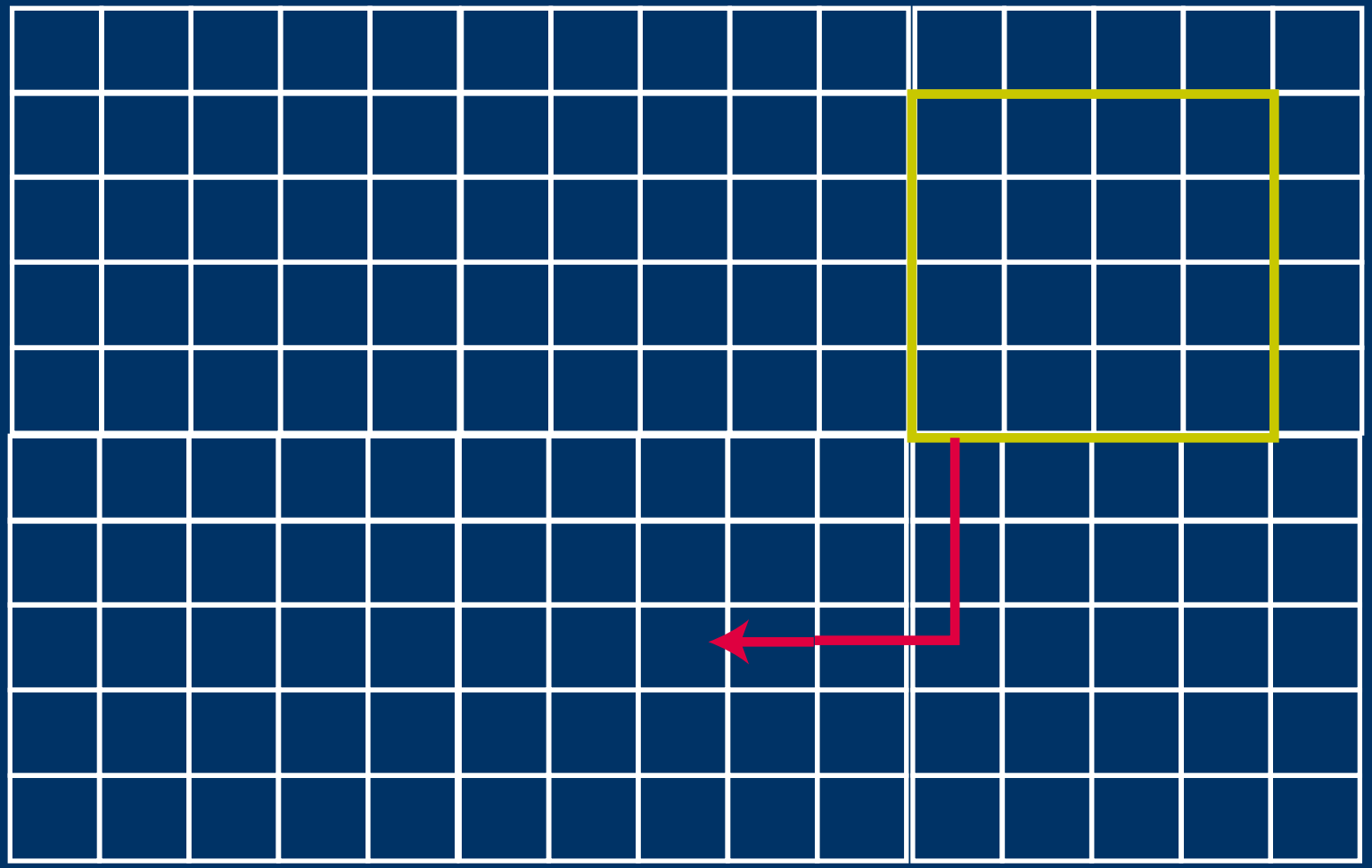


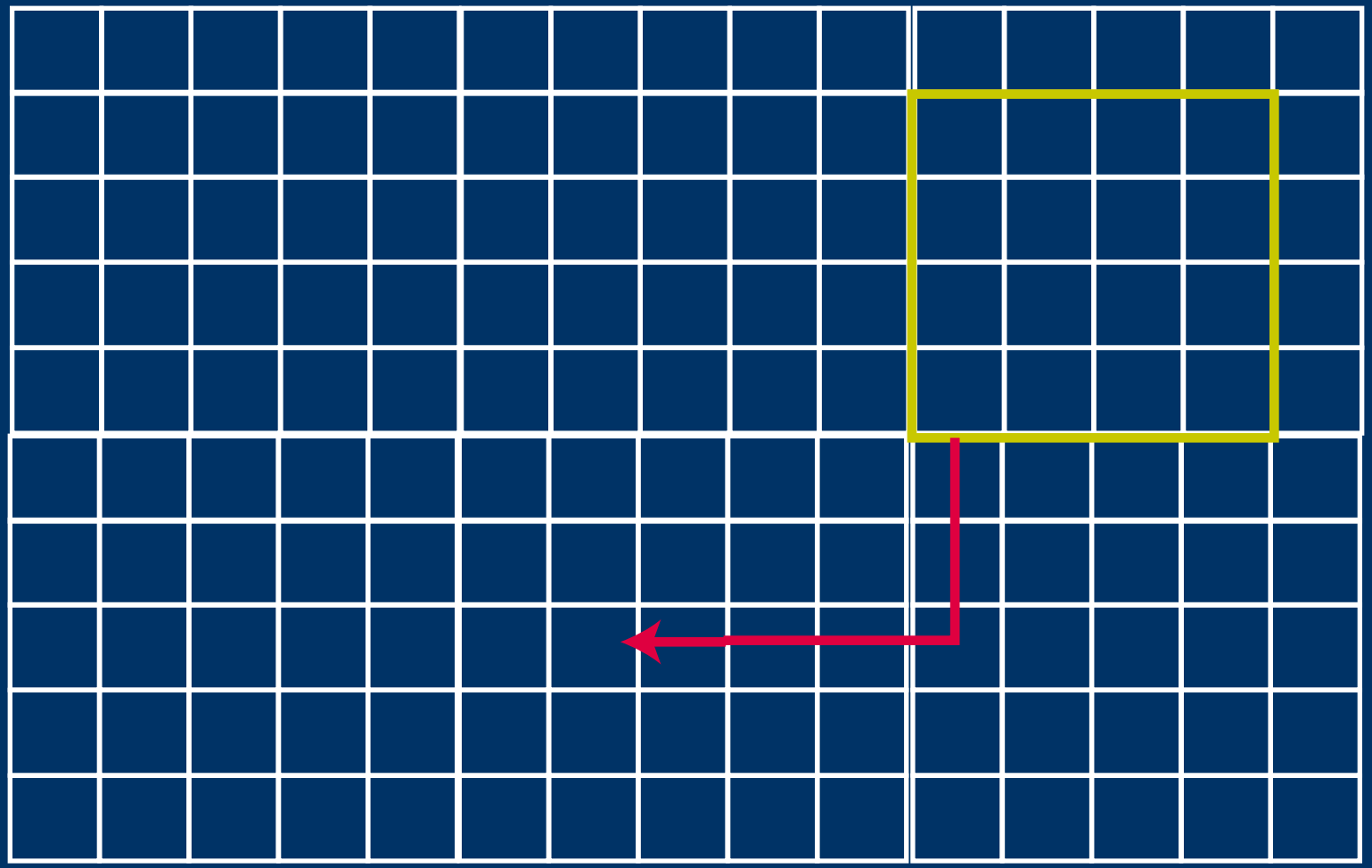
EXAMPLE: HARDWARE LIBRARY



EXAMPLE: HARDWARE LIBRARY



EXAMPLE: HARDWARE LIBRARY



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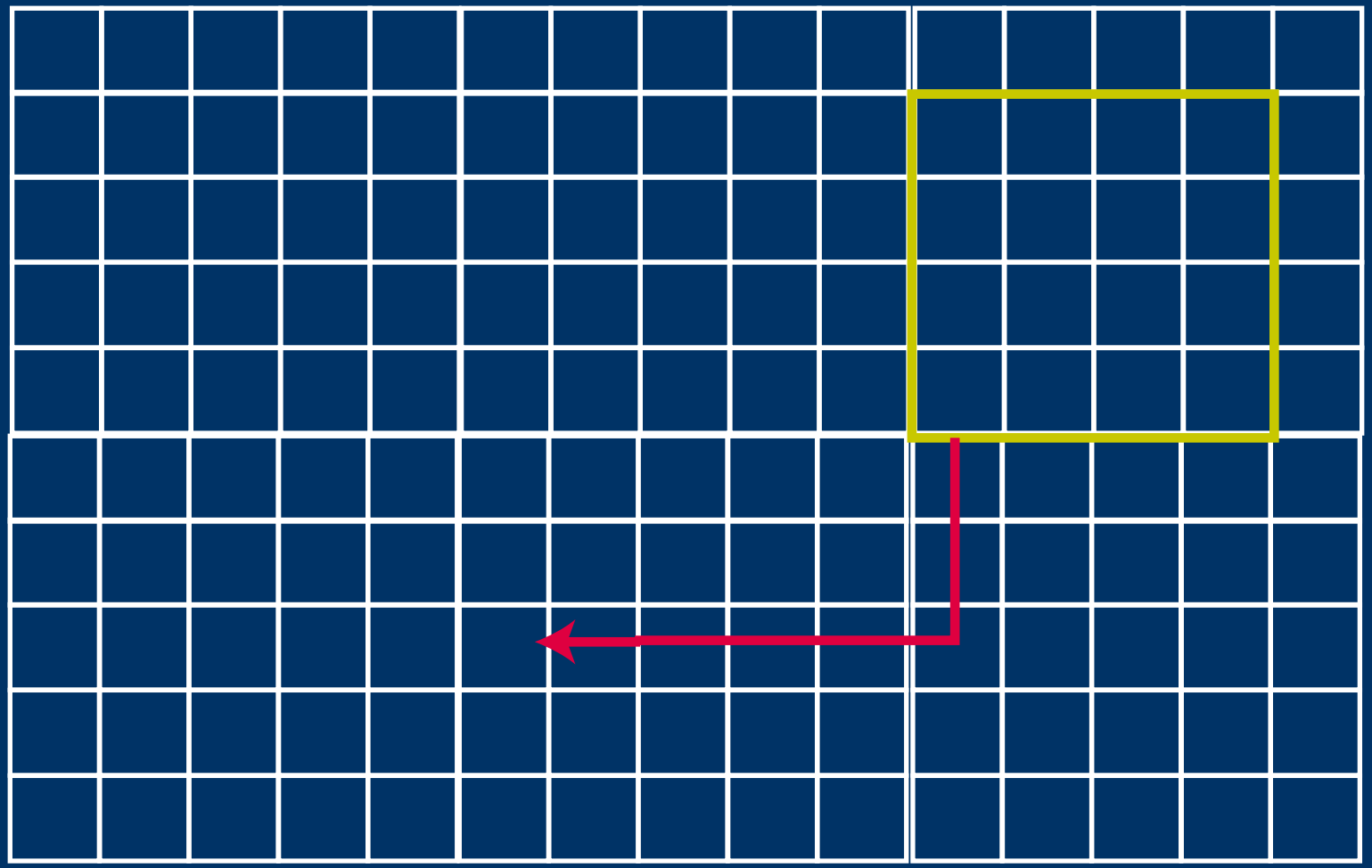

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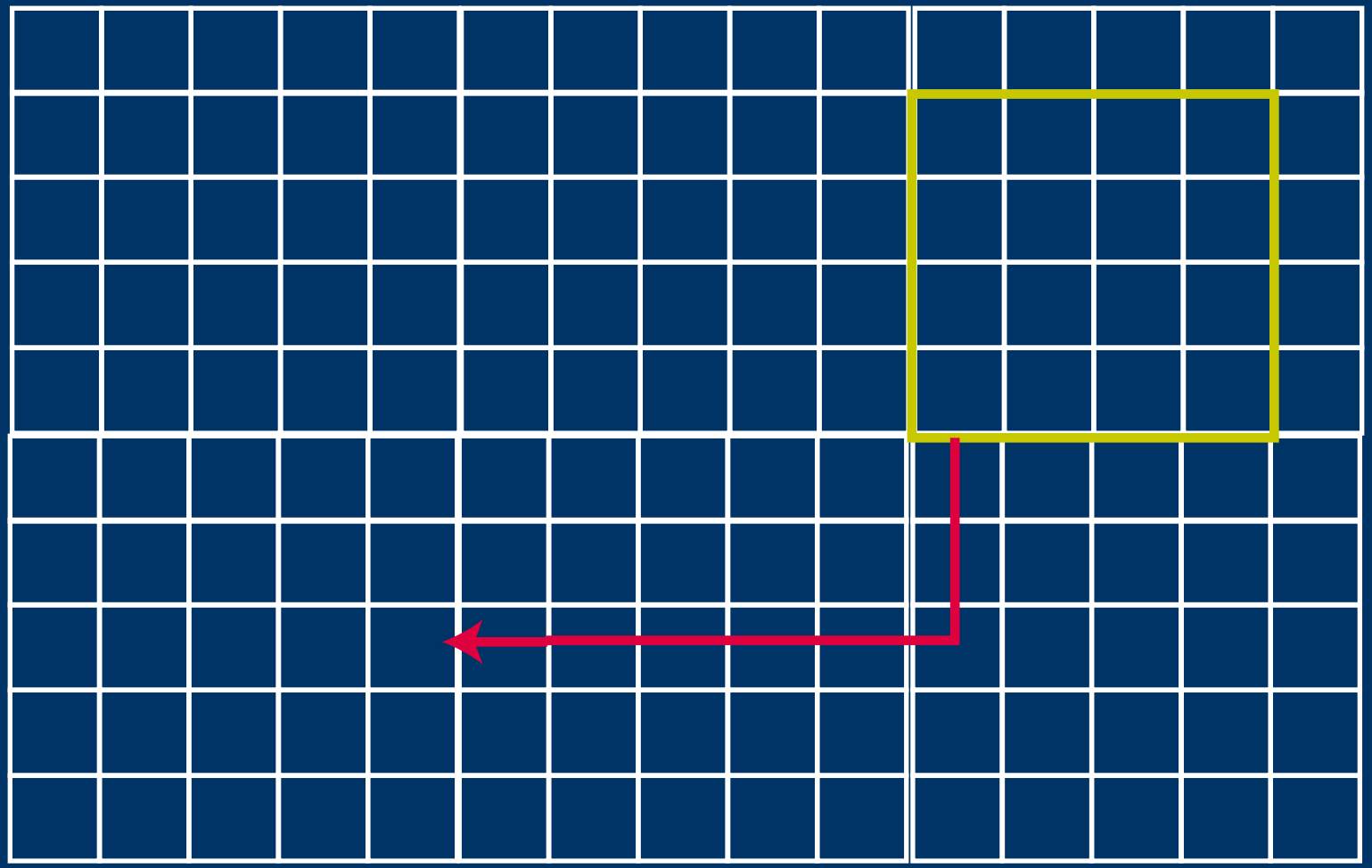

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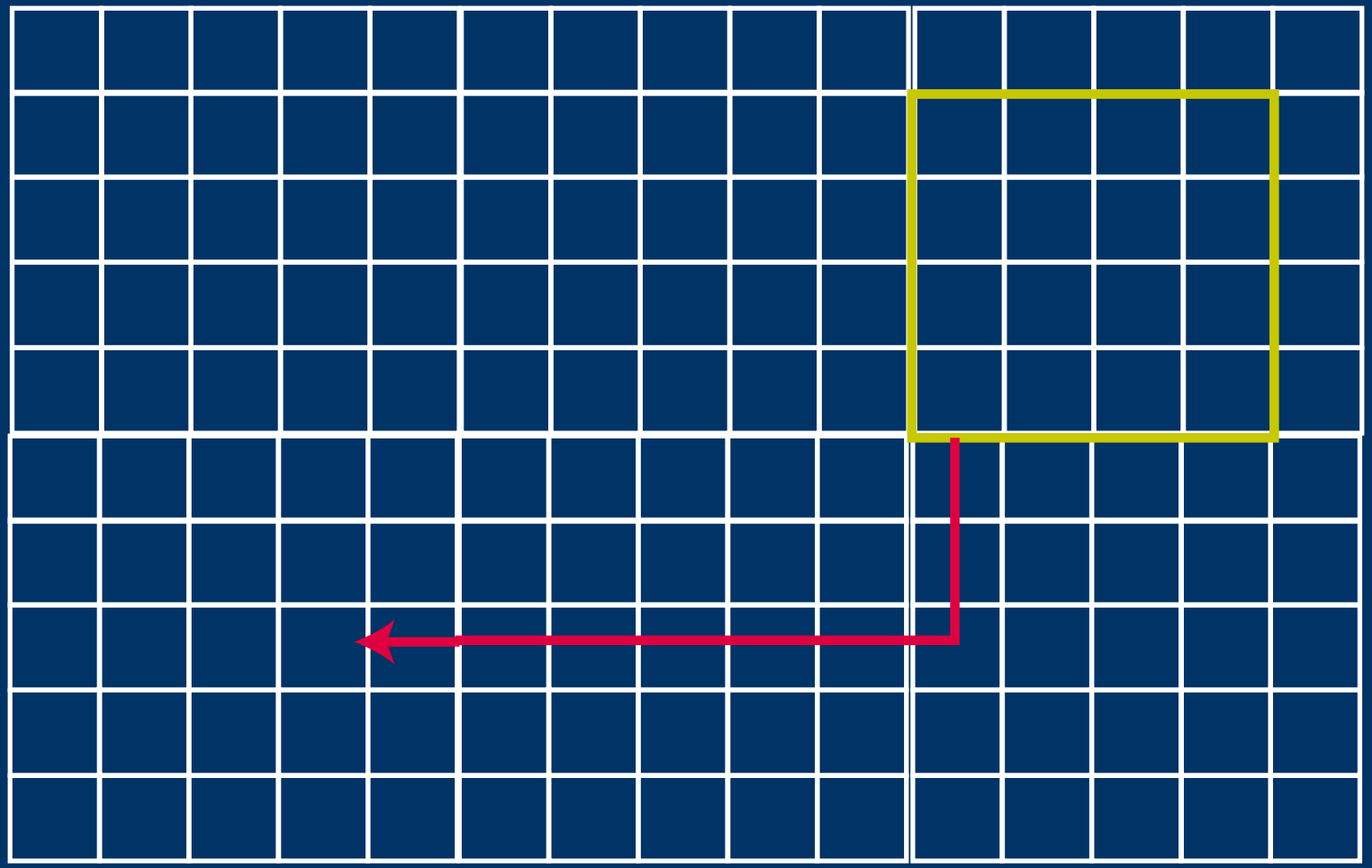

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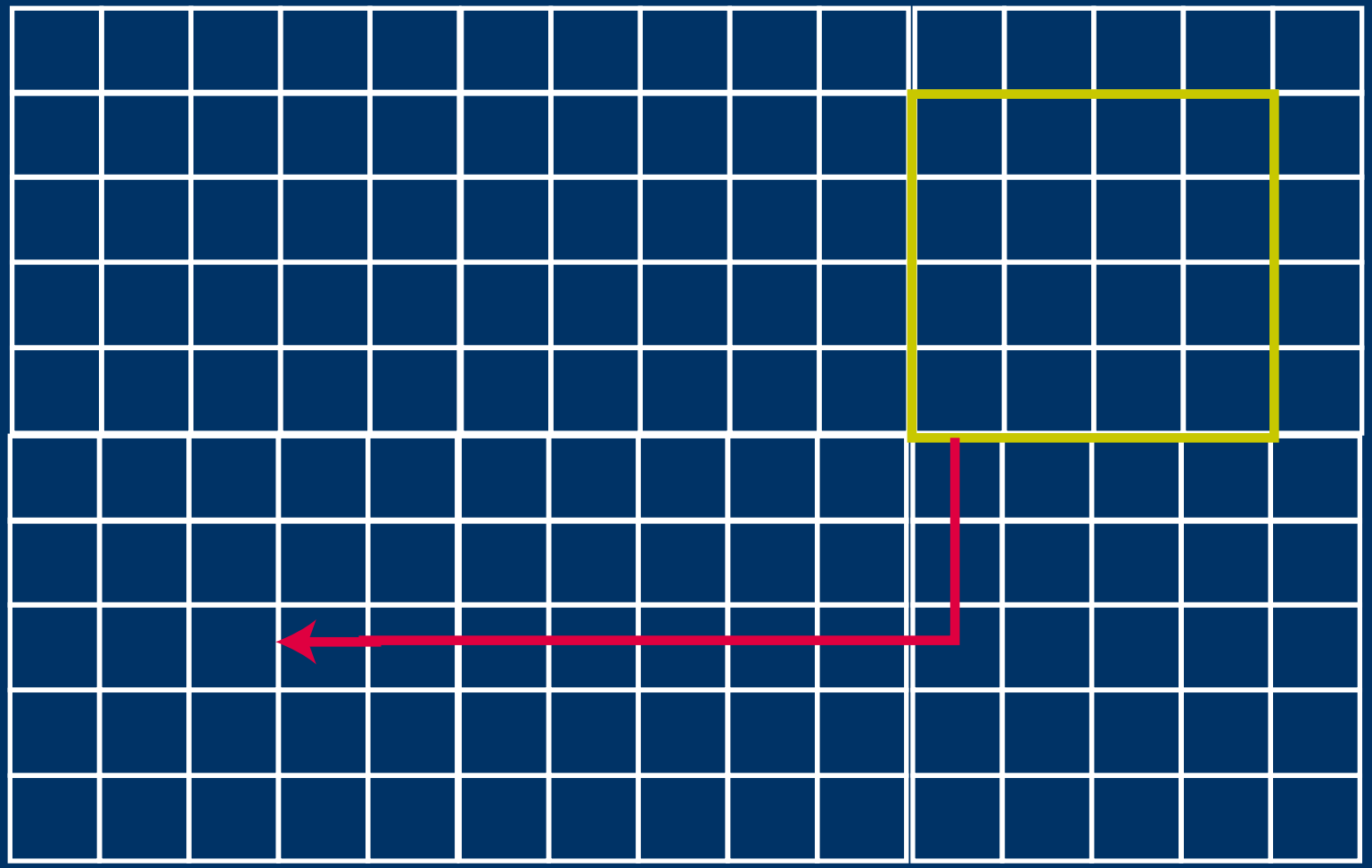

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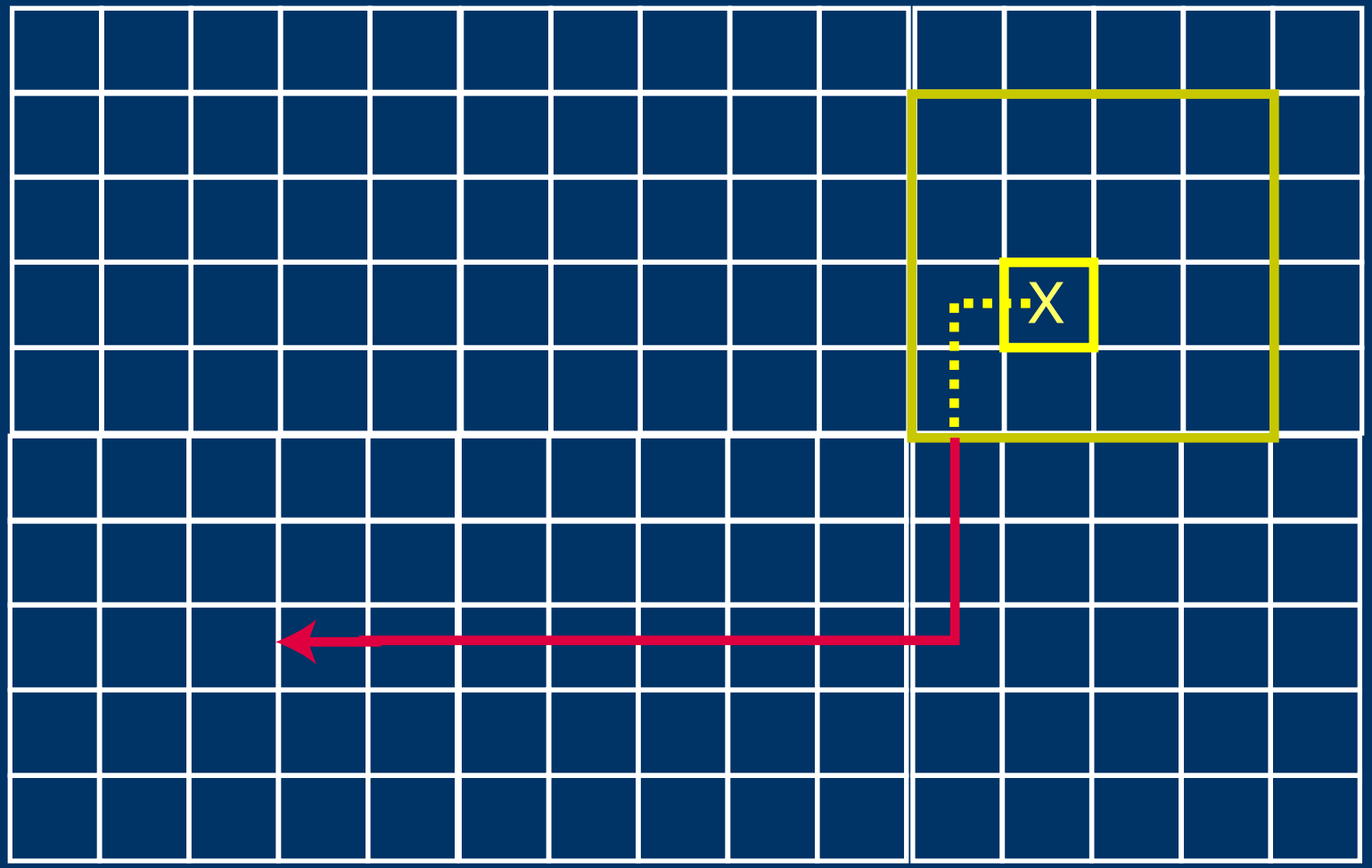
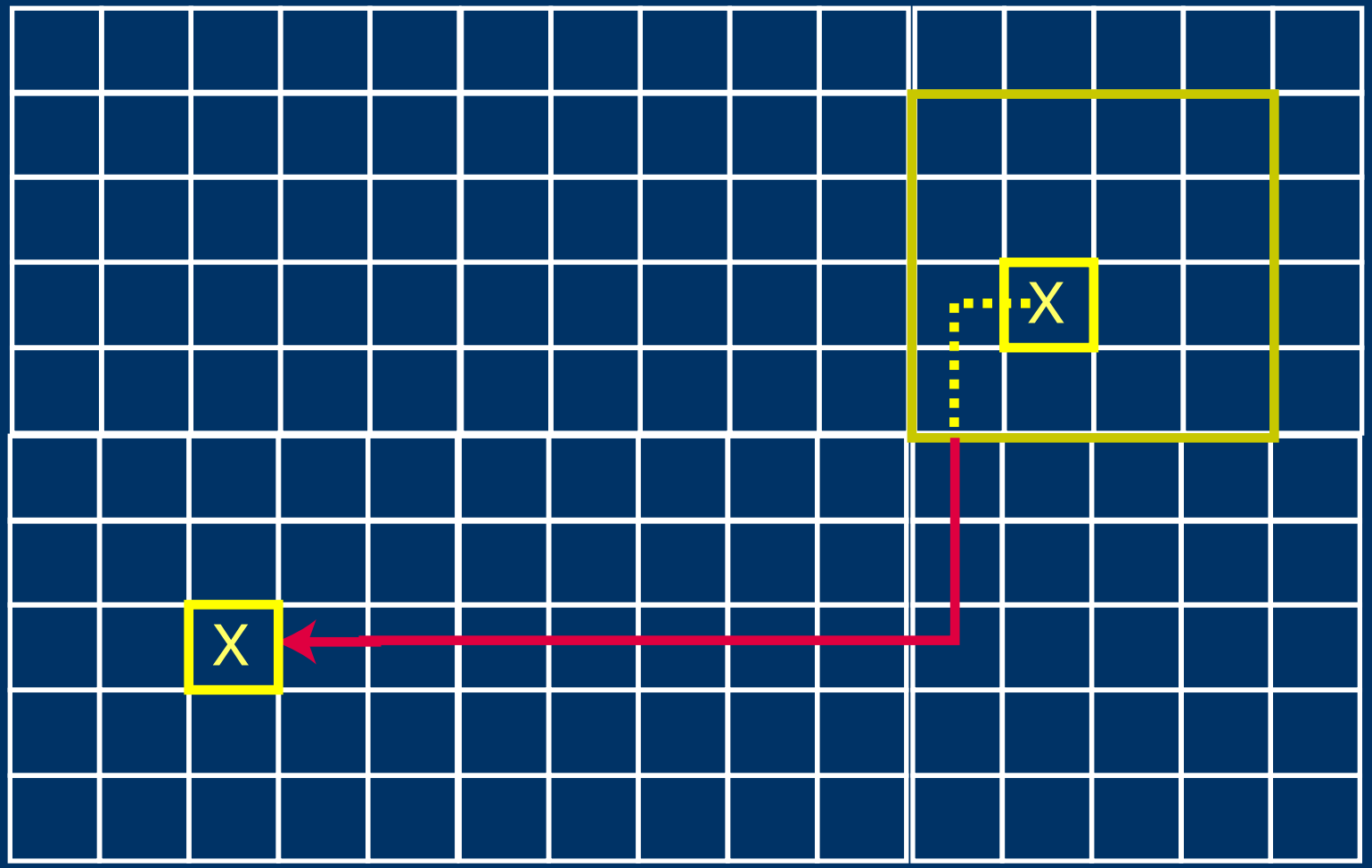


EXAMPLE: HARDWARE LIBRARY



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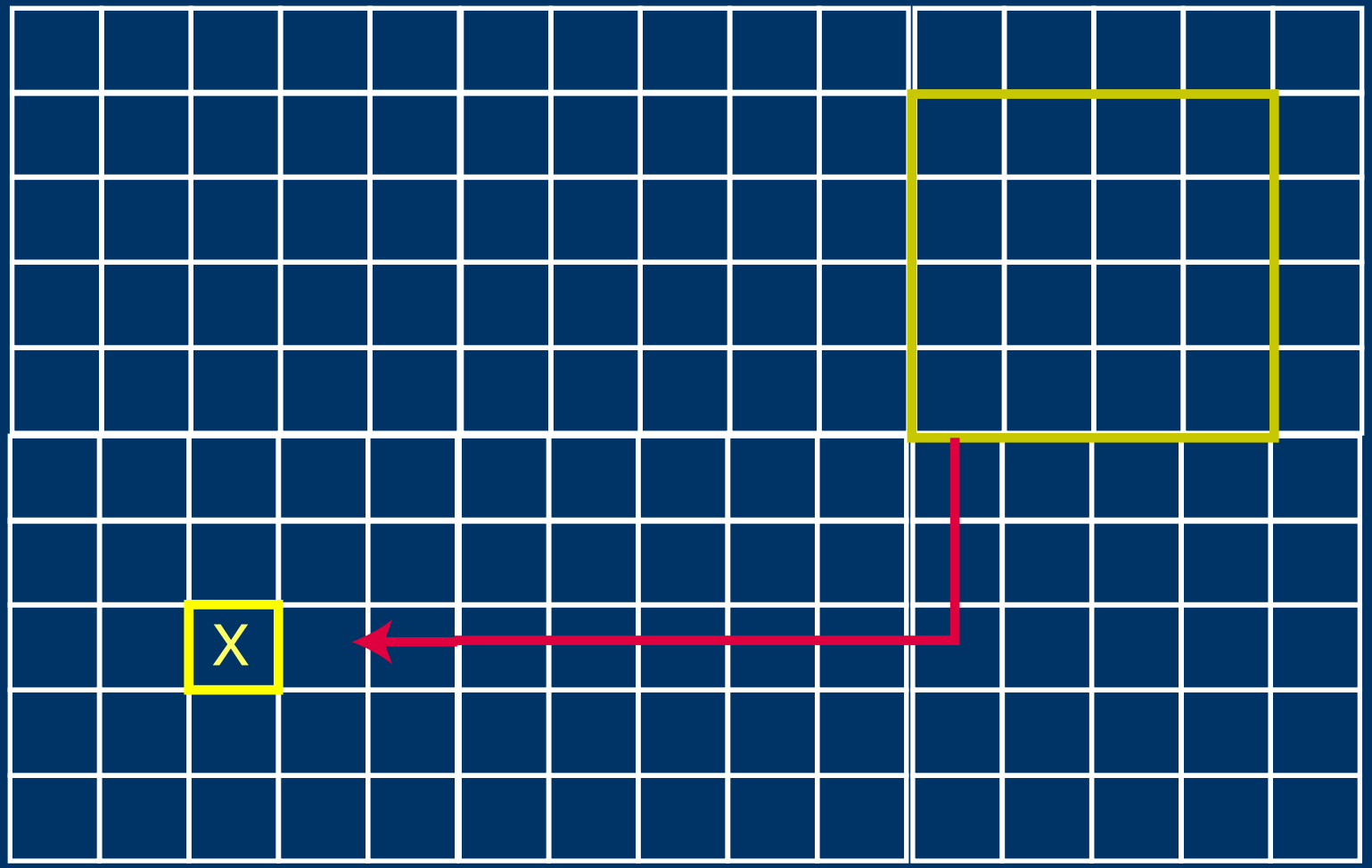

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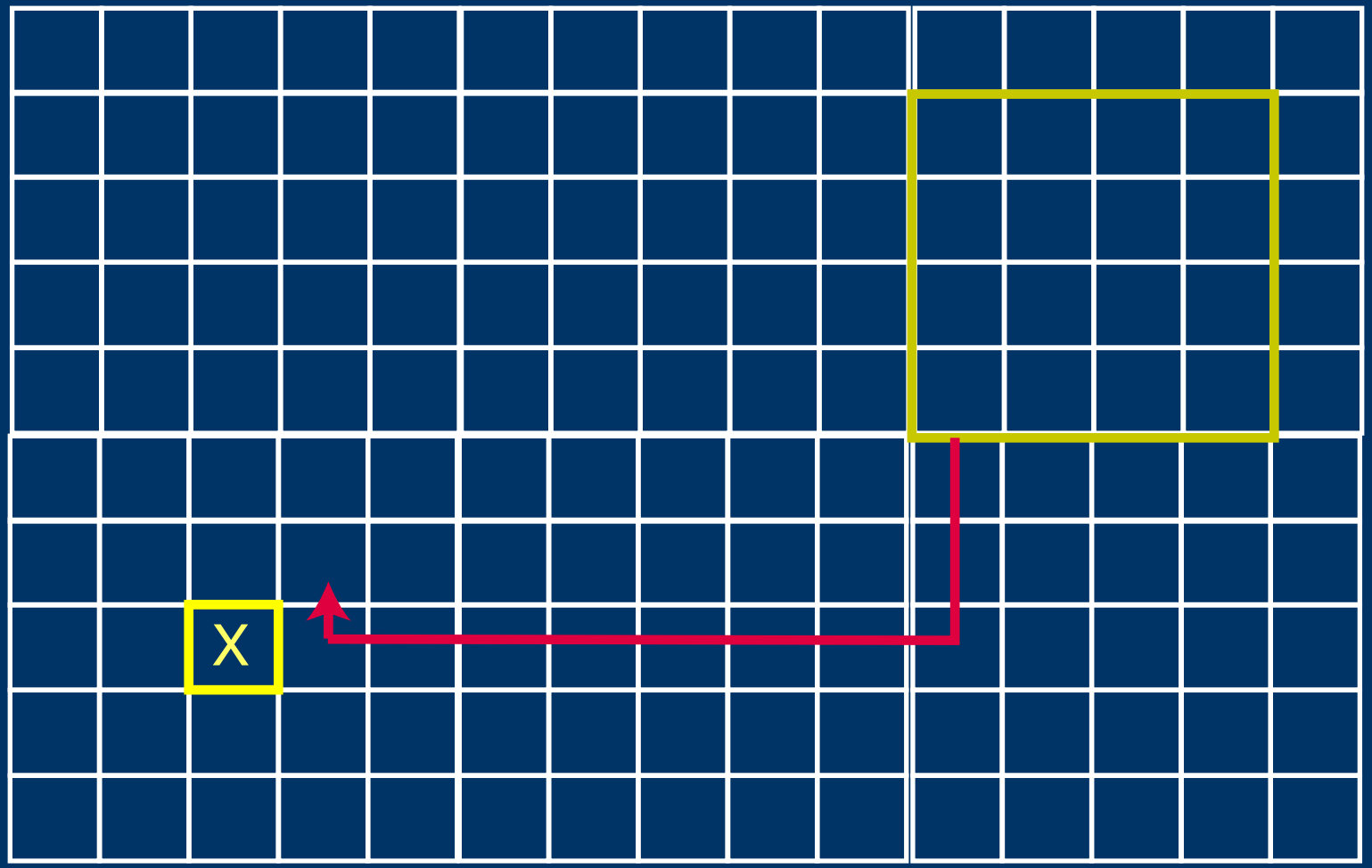

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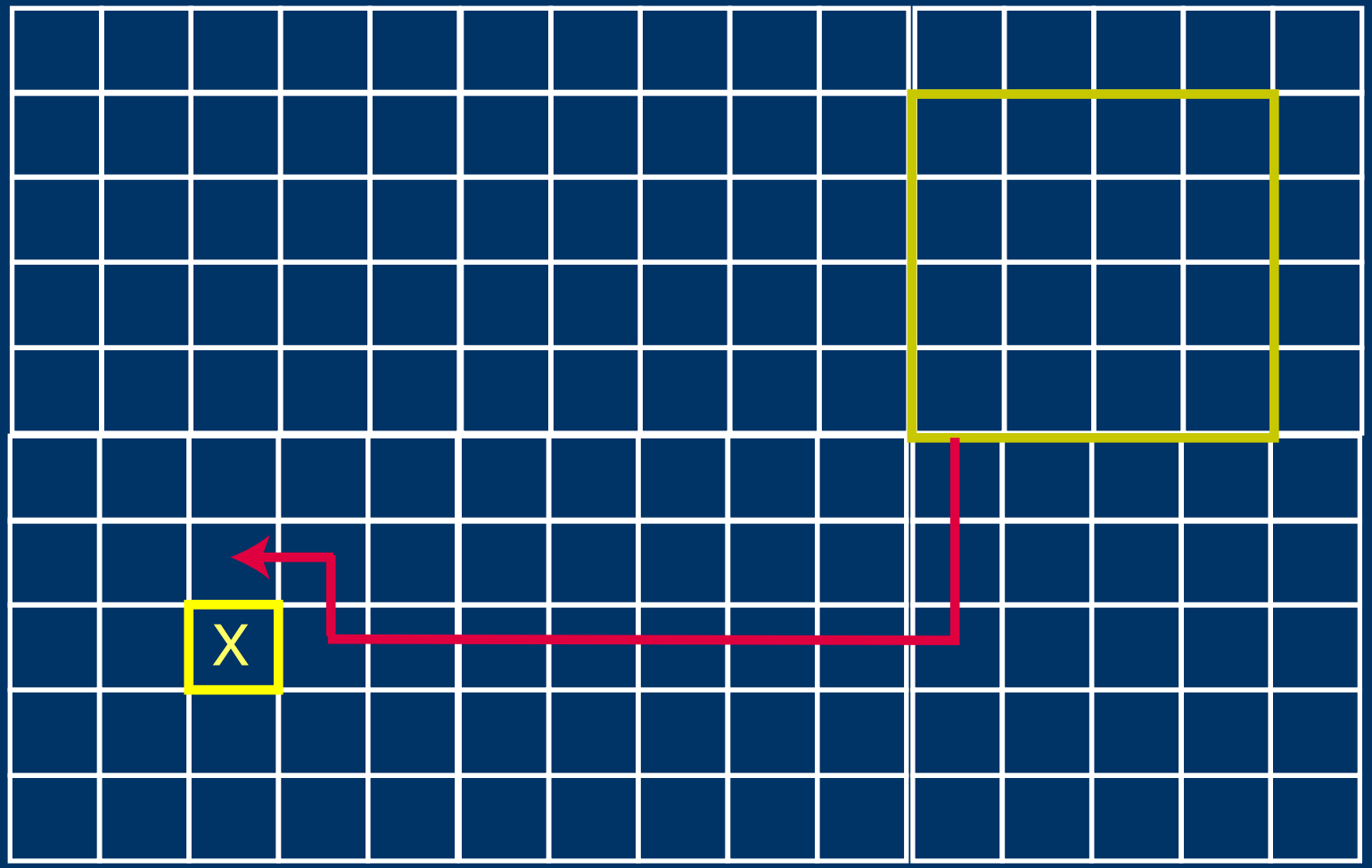

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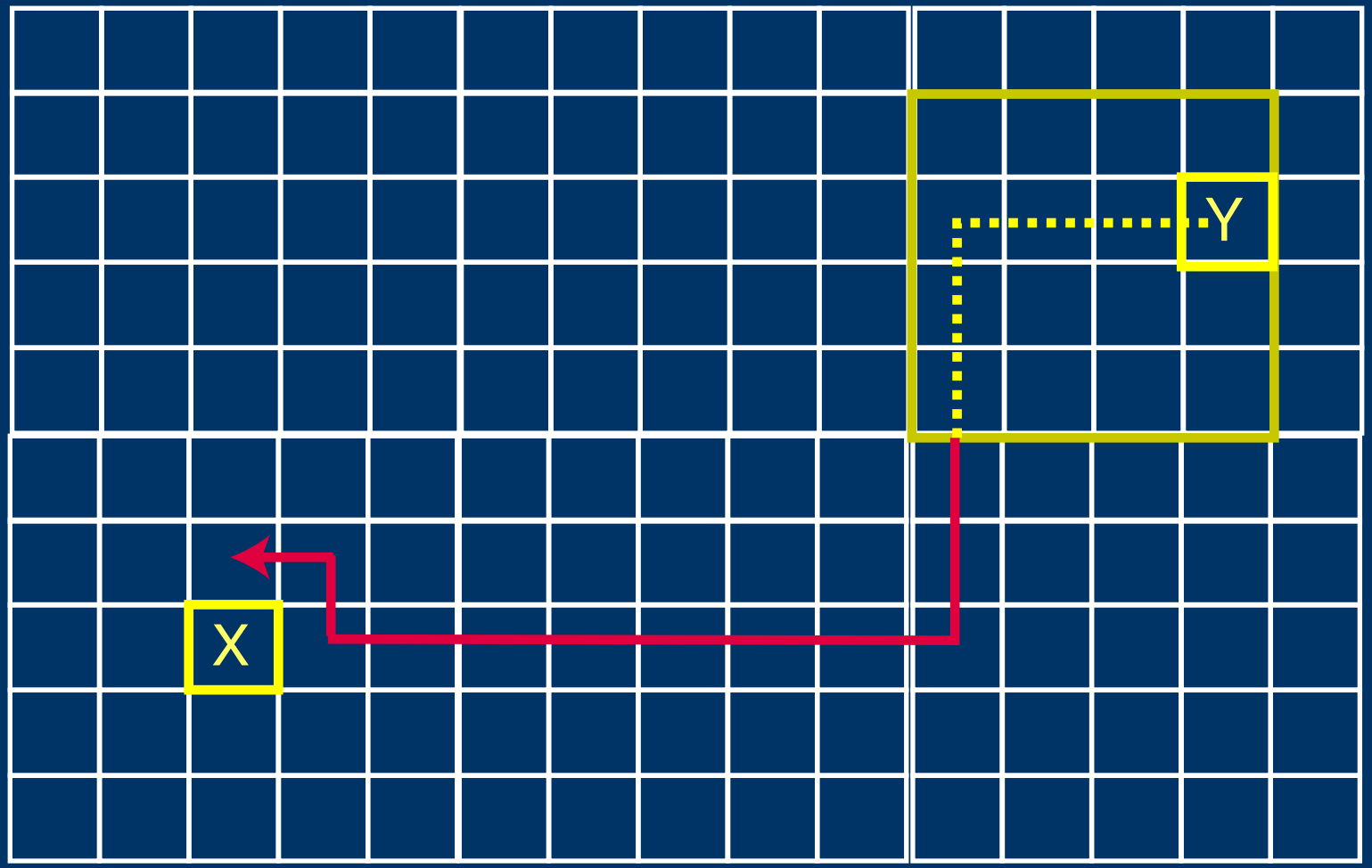

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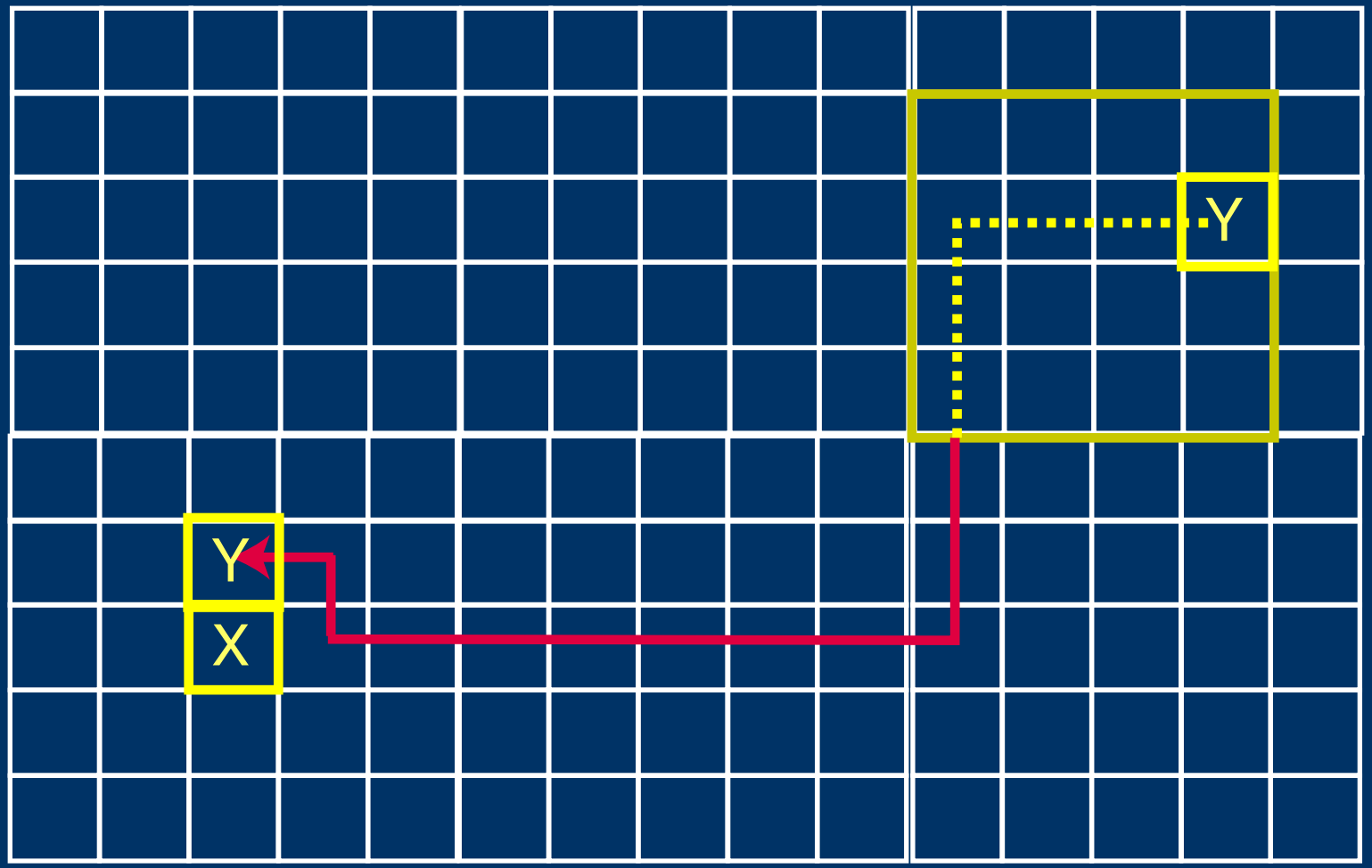

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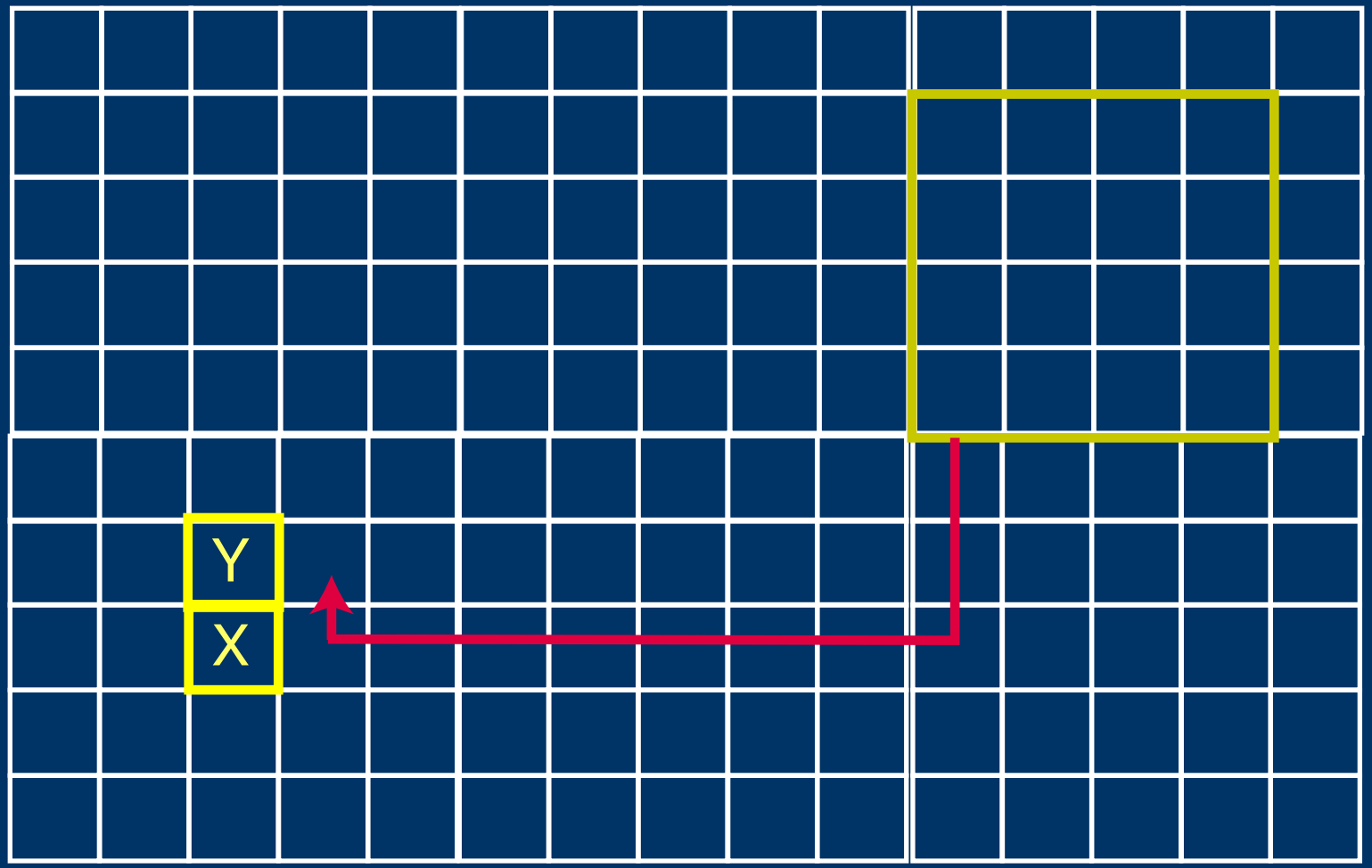
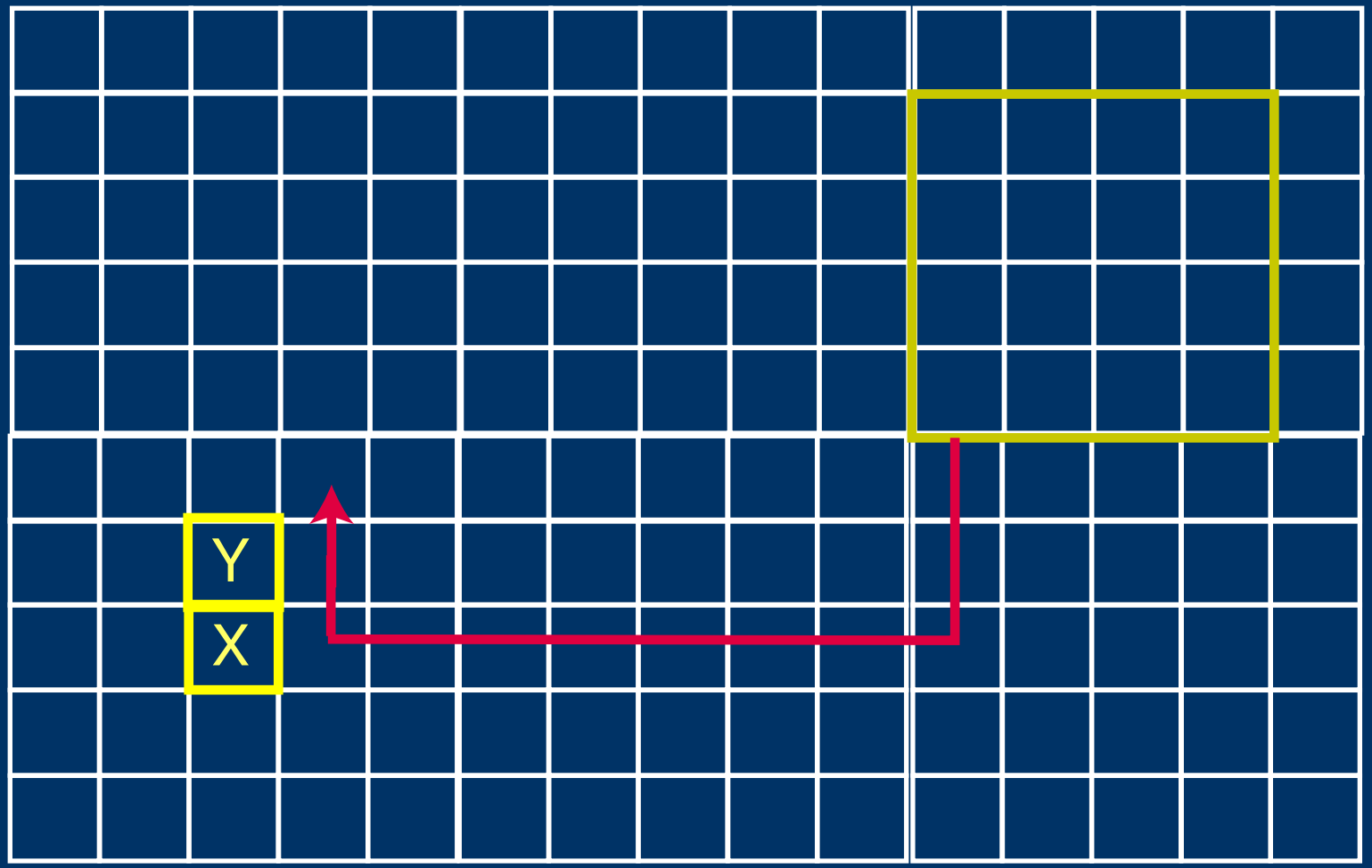


EXAMPLE: HARDWARE LIBRARY



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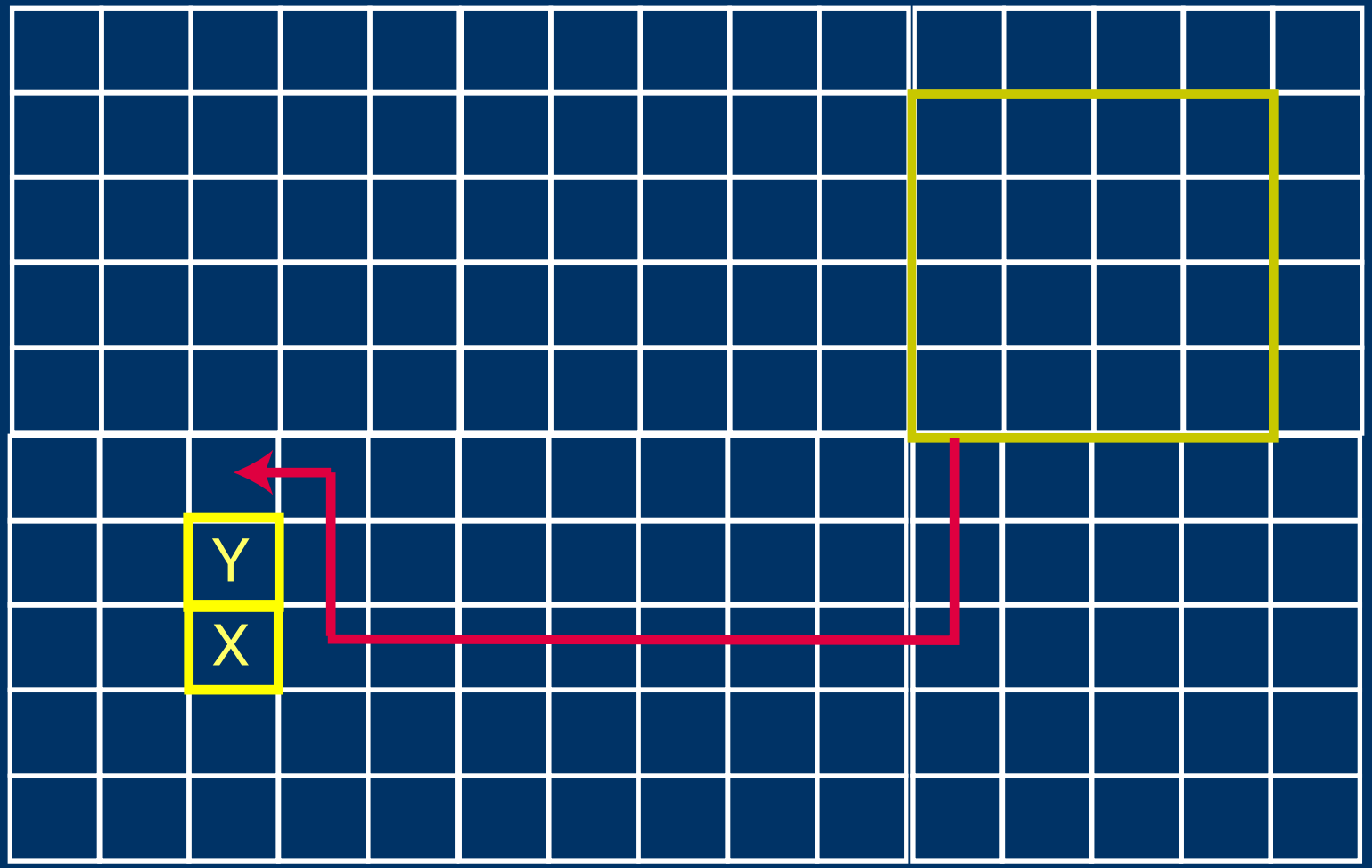

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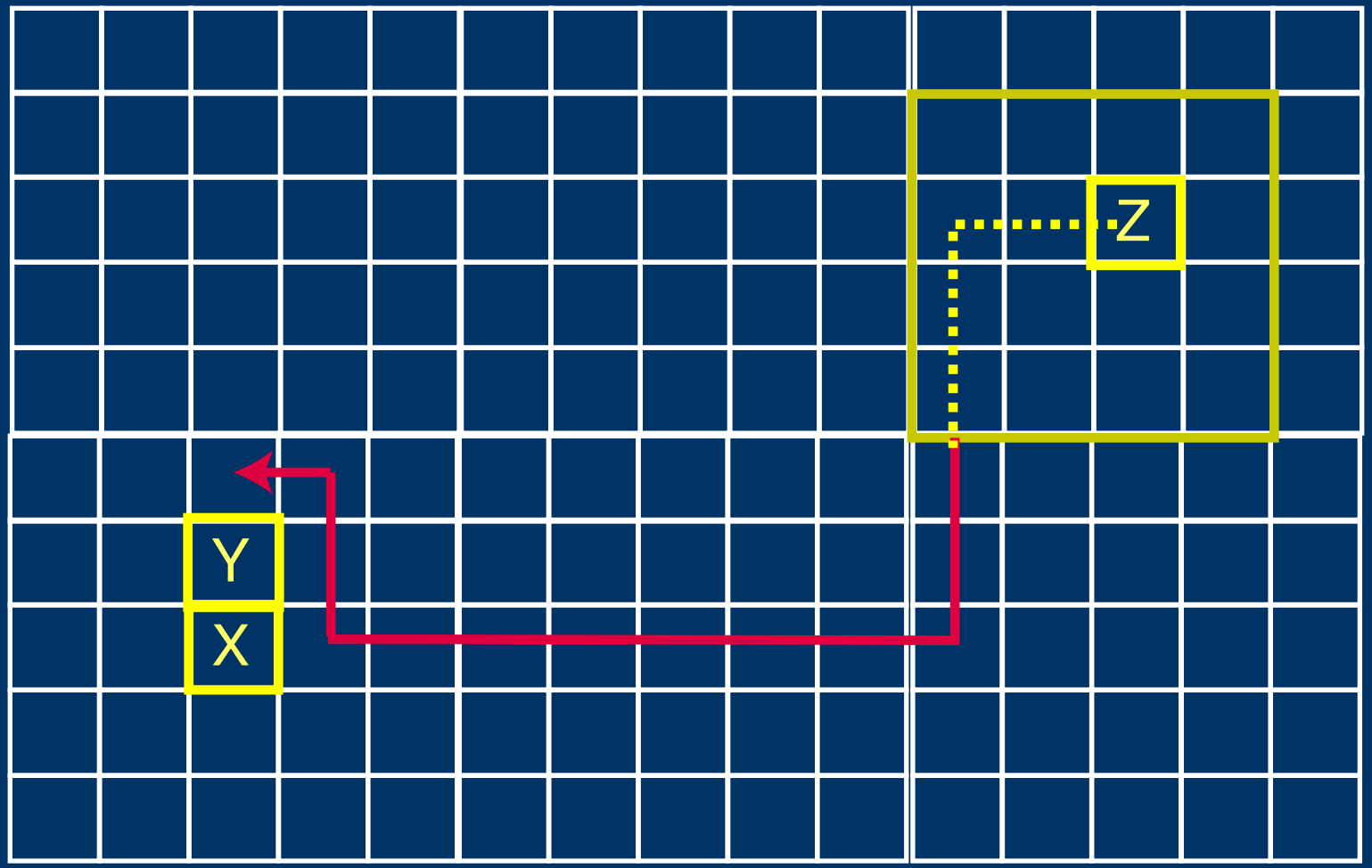

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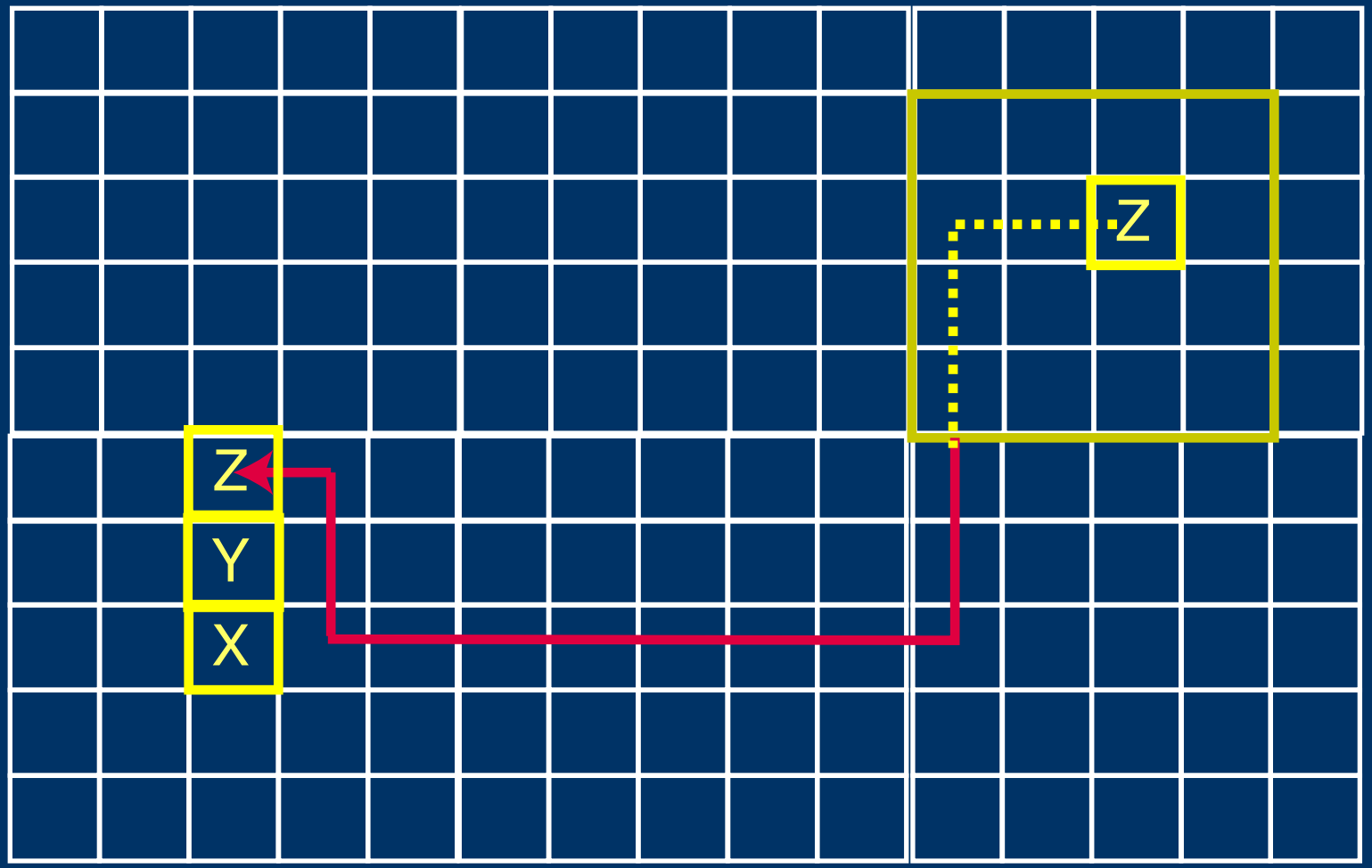


APPLICATION AREAS

APPLICATION AREAS

- General Reconfigurable Platform

APPLICATION AREAS

- General Reconfigurable Platform
- Platform for Dynamic Circuitry
  - On-the-fly SW→HW conversion
  - Evolvable hardware

APPLICATION AREAS

- General Reconfigurable Platform
- Platform for Dynamic Circuitry
- Combined with nanotechnology, could implement Avogadro scale Cell Matrix (Trillion Trillion cells) MASSIVELY Parallel Processor

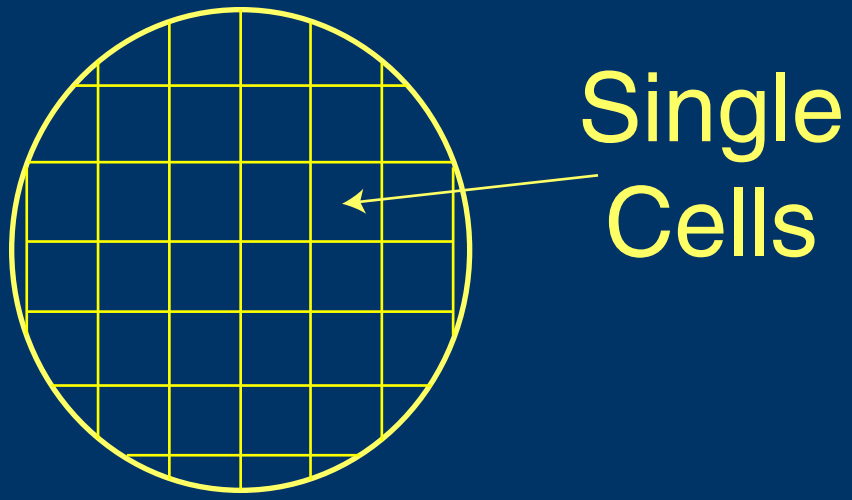
APPLICATION AREAS

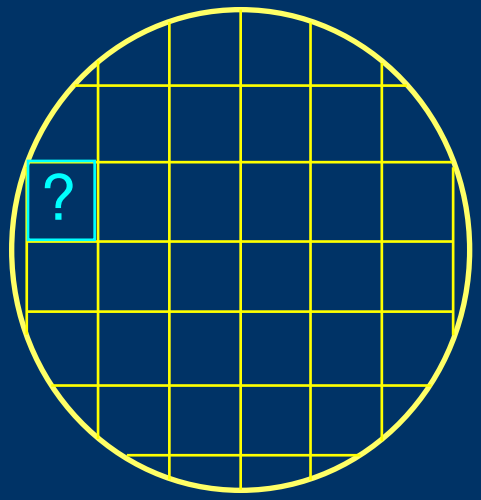
Ultimate Application may be as a Control System

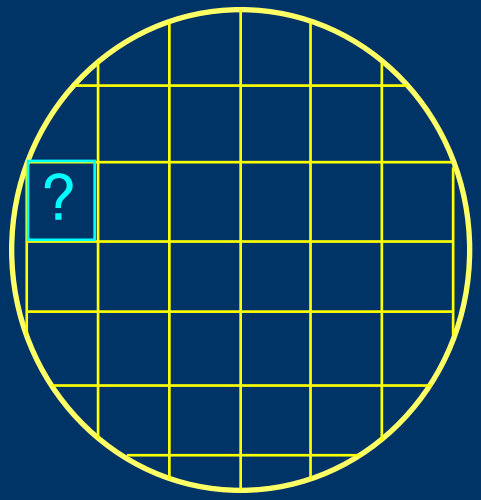
APPLICATIONS TO MANUFACTURING

CELL MATRIX AS A PROCESS DRIVE

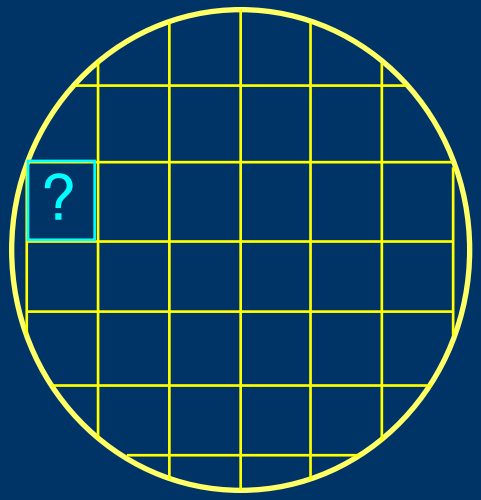
- Fabricate a large Cell Matrix on a new fabrication line
- Cells that work can detect and analyze those that don't
- Useful for debugging the fabrication process itself


Single
Cells

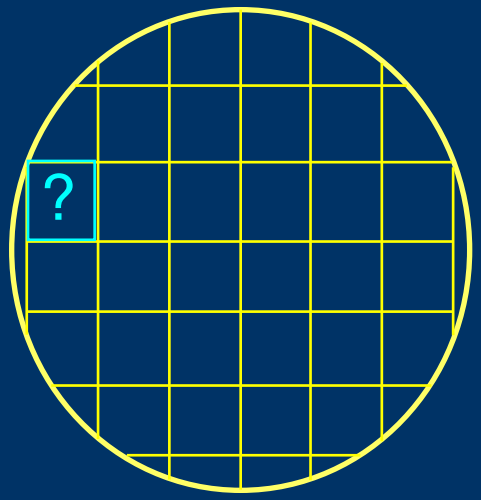




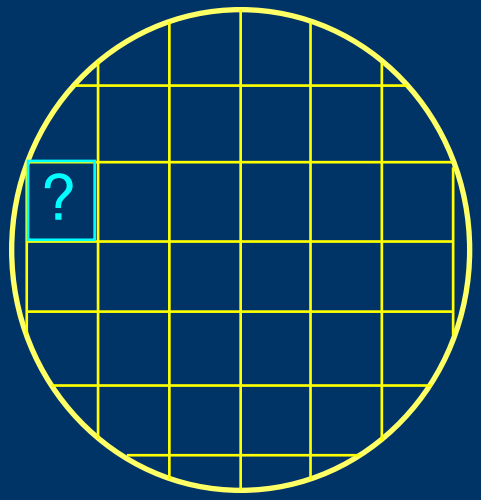
CELL CONFIG	TEST PATTERN	TYPE OF FAULT
Feedback	1010101010	Stuck-at-0 or 1



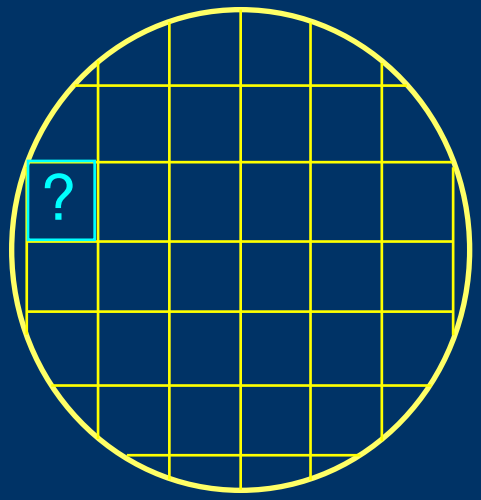
CELL CONFIG	TEST PATTERN	TYPE OF FAULT
Feedback	1010101010	Stuck-at-0 or 1
Inverter	1010101010	Input/Output Short



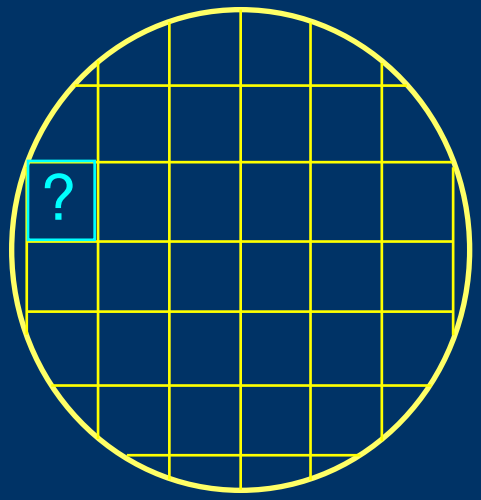
CELL CONFIG	TEST PATTERN	TYPE OF FAULT
Feedback	1010101010	Stuck-at-0 or 1
Inverter	1010101010	Input/Output Short
000000000...	Read back TT	TT Stuck-at-1



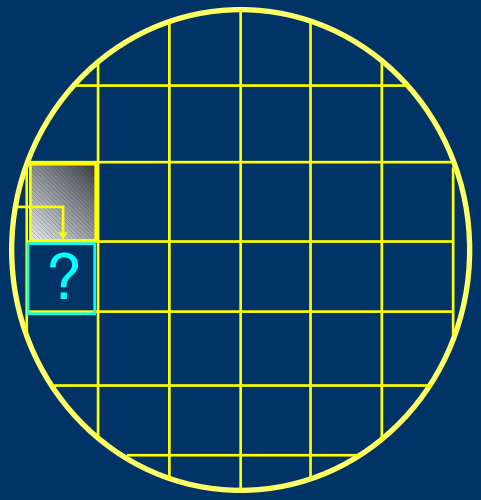
CELL CONFIG	TEST PATTERN	TYPE OF FAULT
Feedback	1010101010	Stuck-at-0 or 1
Inverter	1010101010	Input/Output Short
000000000...	Read back TT	TT Stuck-at-1
1111111111...	Read back TT	TT Stuck-at-0

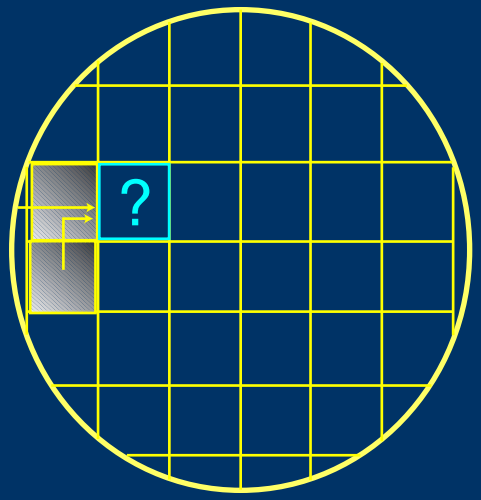


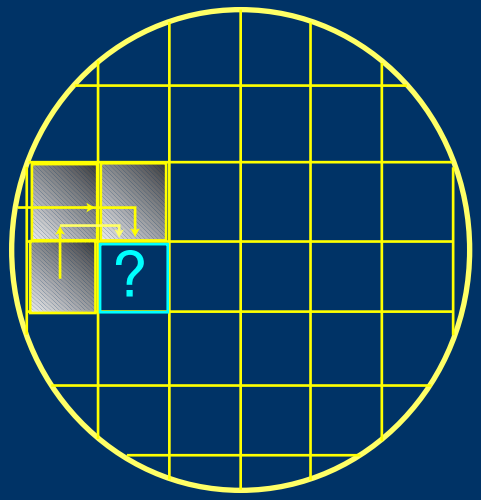
CELL CONFIG	TEST PATTERN	TYPE OF FAULT
Feedback	1010101010	Stuck-at-0 or 1
Inverter	1010101010	Input/Output Short
000000000...	Read back TT	TT Stuck-at-1
111111111...	Read back TT	TT Stuck-at-0
101010101...	Read Back TT	TT Column Short

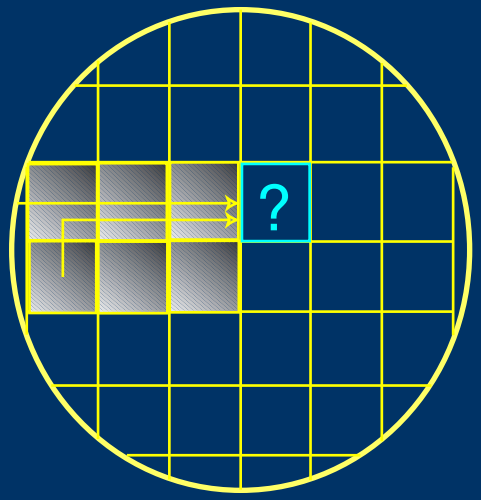


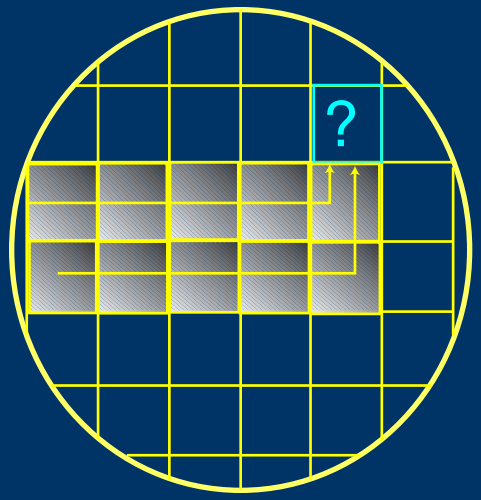
CELL CONFIG	TEST PATTERN	TYPE OF FAULT
Feedback	1010101010	Stuck-at-0 or 1
Inverter	1010101010	Input/Output Short
000000000...	Read back TT	TT Stuck-at-1
111111111...	Read back TT	TT Stuck-at-0
101010101...	Read Back TT	TT Column Short
1111111100 000000111...	Read back TT	TT Row Short

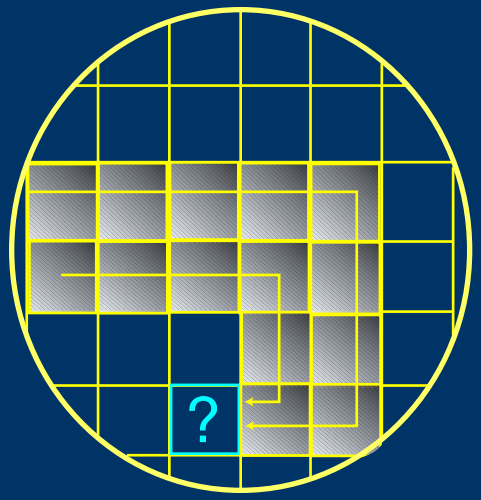












TESTBED FOR RADHARD FABRICATION

- Run these self-analyzing circuits while exposed to high radiation
- Can compare different types of shielding in real-time
- Can correct soft errors to allow continued testing

PERFECTLY USABLE CHIPS DESPITE IMPERFECT FABRICATION

- Normally use two bins: GOOD and BAD
- With a Cell Matrix, can have *grades* of chips (99%, 80%, 40%)
- Can sell chips while you're still refining your fab

WAFER SCALE INTEGRATION

- Defects are usual show stopper
- There are specialized architectures that address this issue
- The Cell Matrix is a **completely general purpose** architecture that addresses this issue

STACKED DIE/ 3D ASSEMBLY

- Traditionally, this can involve mehanical alignment problems
- With a Cell Matrix, don't need perfect alignment
- Stack first, then use system to analyze and correct alignment errors

INTERLACE CELLS WITH OTHER DIE ON A WAFER

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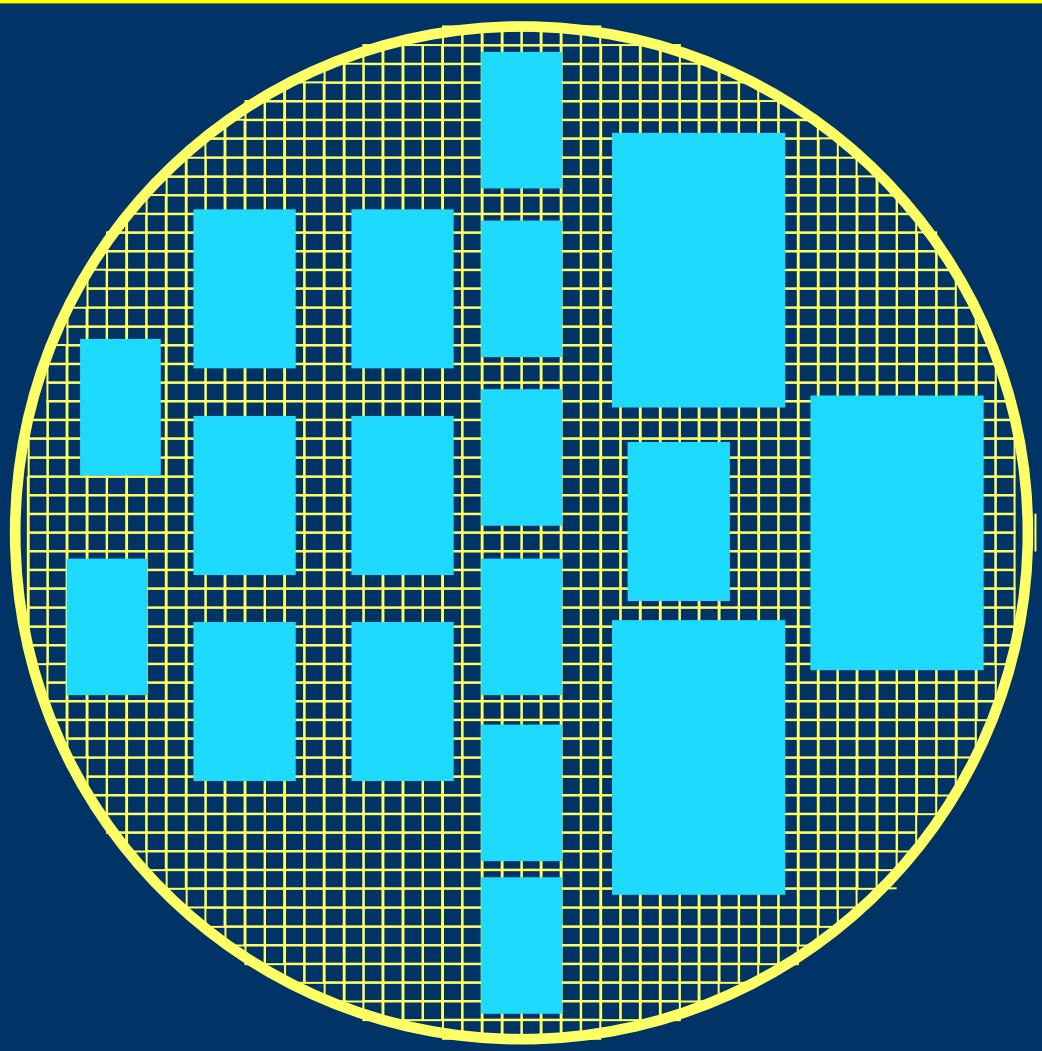

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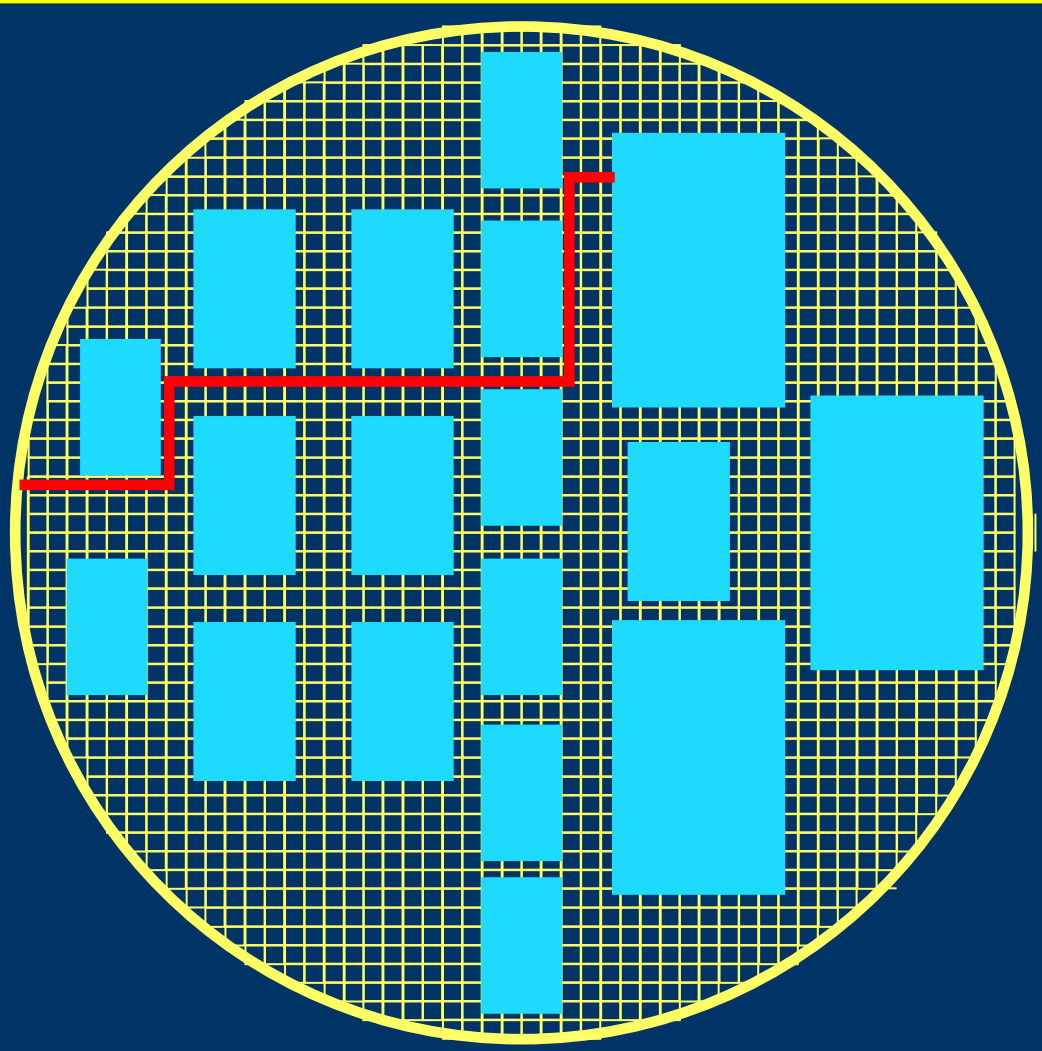

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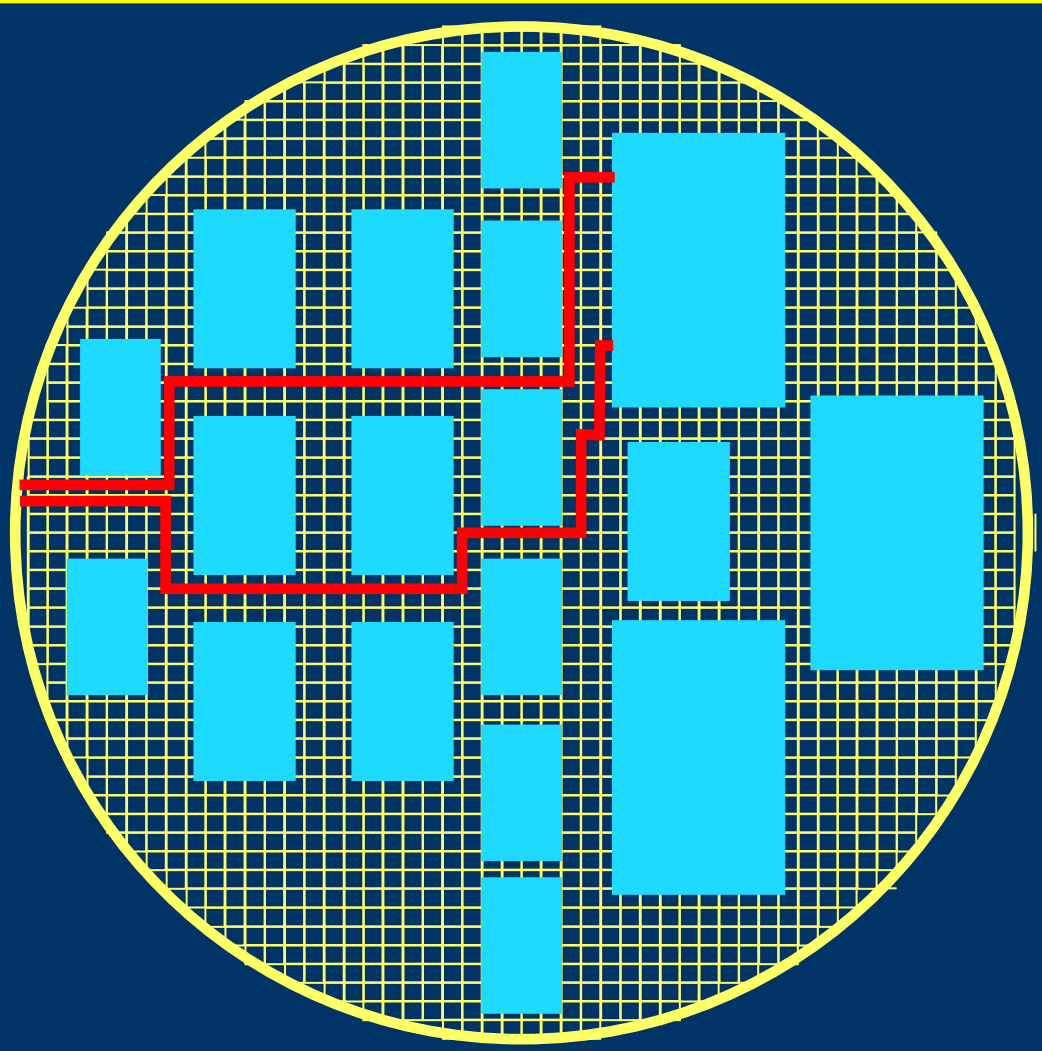

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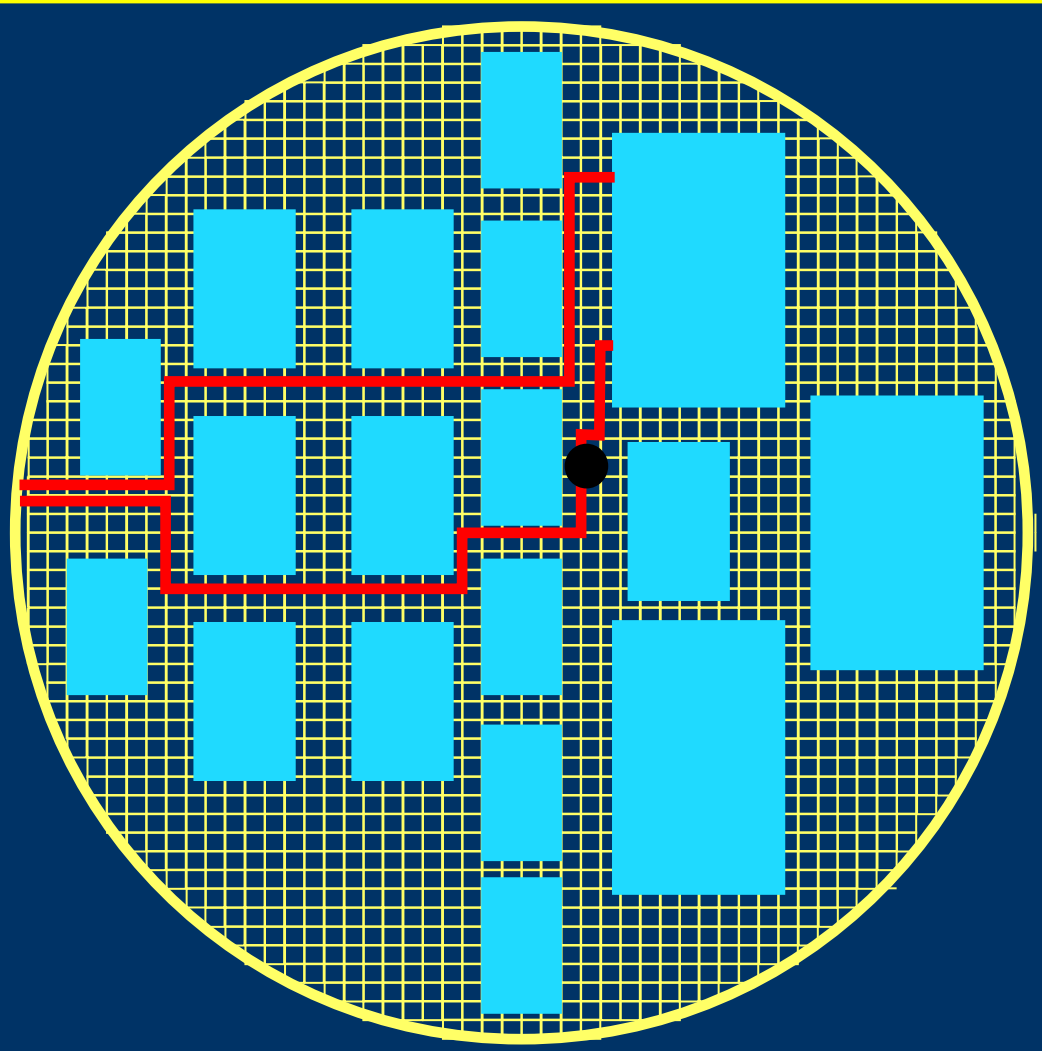

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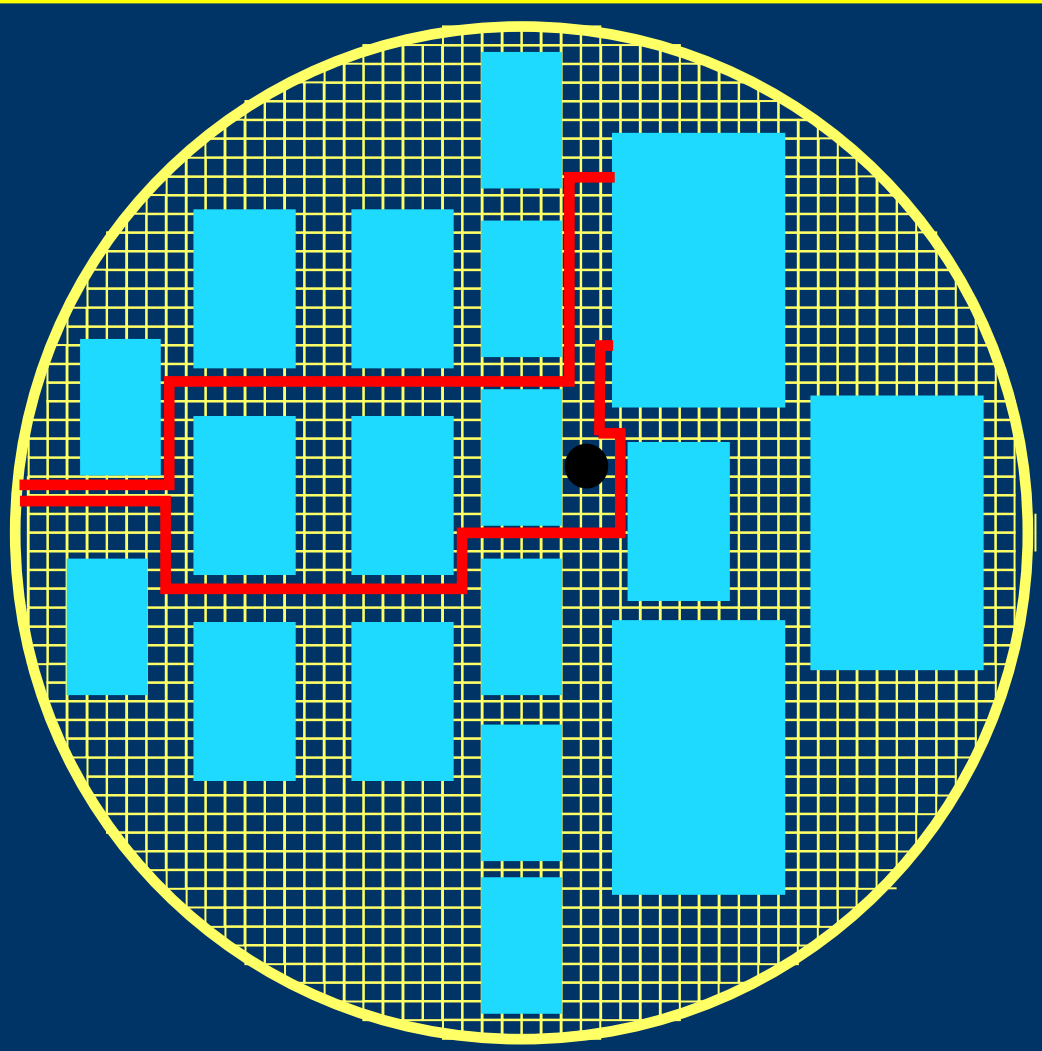

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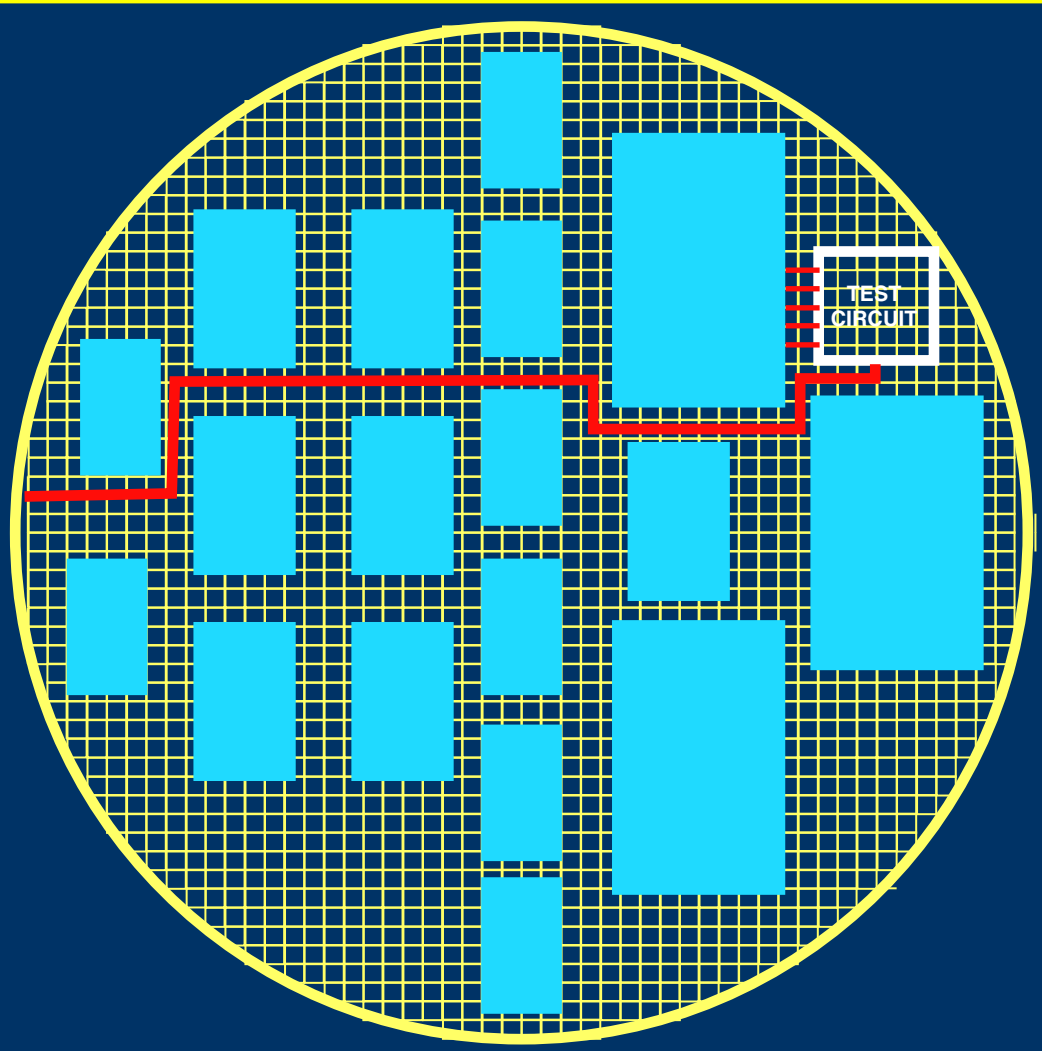

SUMMARY

- Simple, scalable, self configurable architecture
- Circuits that process both Data and Circuits
- Well suited to numerous manufacturing-related tasks

FOR MORE INFORMATION...

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(877) 473-0882
nmacias@cellmatrix.com